JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1

Thermal Sensor
SMSC
EMC2103 27

CLK GEN.
ICS9LPRS365B 3

Intel CPU
Penryn SFF 4,5,6

HOST BUS
667/800/1066MHz@1.05V

DDR3
800/1066 MHz 17,18

DDR3
800/1066 MHz 17,18

Cantiga-GS SFF
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
7,8,9,10,11,12

X4 DMI
400MHz

C-Link0

UMA LVDS
UMA CRT
DIS LVDS
DIS CRT

Switchable Graphic 40, 41

LVDS

LCD 19

RGB CRT

VRAM(DDR3)
64Mbx16x4 (512MB) 57

PCIe x 16

ATI M92-S2 53,54,55,56

HDMI

CRT BD 20

CRT

HDMI

ICH9M SFF
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
13,14,15,16

LAN
Giga LAN
Atheros AR8131

TXFM

RJ45

23
INT.SPKR
1.5W

Int MIC
19

Codec
Realtek
ALC269Q 22

AZALIA

Line Out

MIC In

CRT
BD
20

SATA

PCIe x1 *3port

MINI BD
USB 3 Port
25

Mini 1 Card
WLAN

Mini 2 Card
3G

LPC BUS

USB

SATA
HDD SATA

SATA
ODD SATA

CARDREADER
BD 24

SATA
SSD/HDD SATA 21

CRT BD
2 Port 20

POWER BD
1 Port 26

CARDREADER BD
2 Port 24

Camera 17

MINI BD
3 Port 25

USB Blue Tooth 24

KBC
Winbond
WPCE773LA0DG 28

SPI

BIOS
(2MB) 29

Touch Pad 30

INT. KB 28

LPC
DEBUG
CONN.

MS/MS Pro/xD
/MMC/SD

PCB STACKUP

TOP	L1
S	L2
VCC/GND	L3
S	L4
VCC/GND	L5
GND/VCC	L6
S	L7
BOTTOM	L8

SYSTEM DC/DC
TPS51125 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8202 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)

RT8202 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)

RT9026 39

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)

CHARGER
MAX8731A 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC
ADP3207A 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A

VGA
ISL6263A 40

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

DIS

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Title: BLOCK DIAGRAM
Size: Custom
Document Number: JM41_Discrete
Rev: -2
Date: Tuesday, April 28, 2009
Sheet 1 of 48

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

DIS

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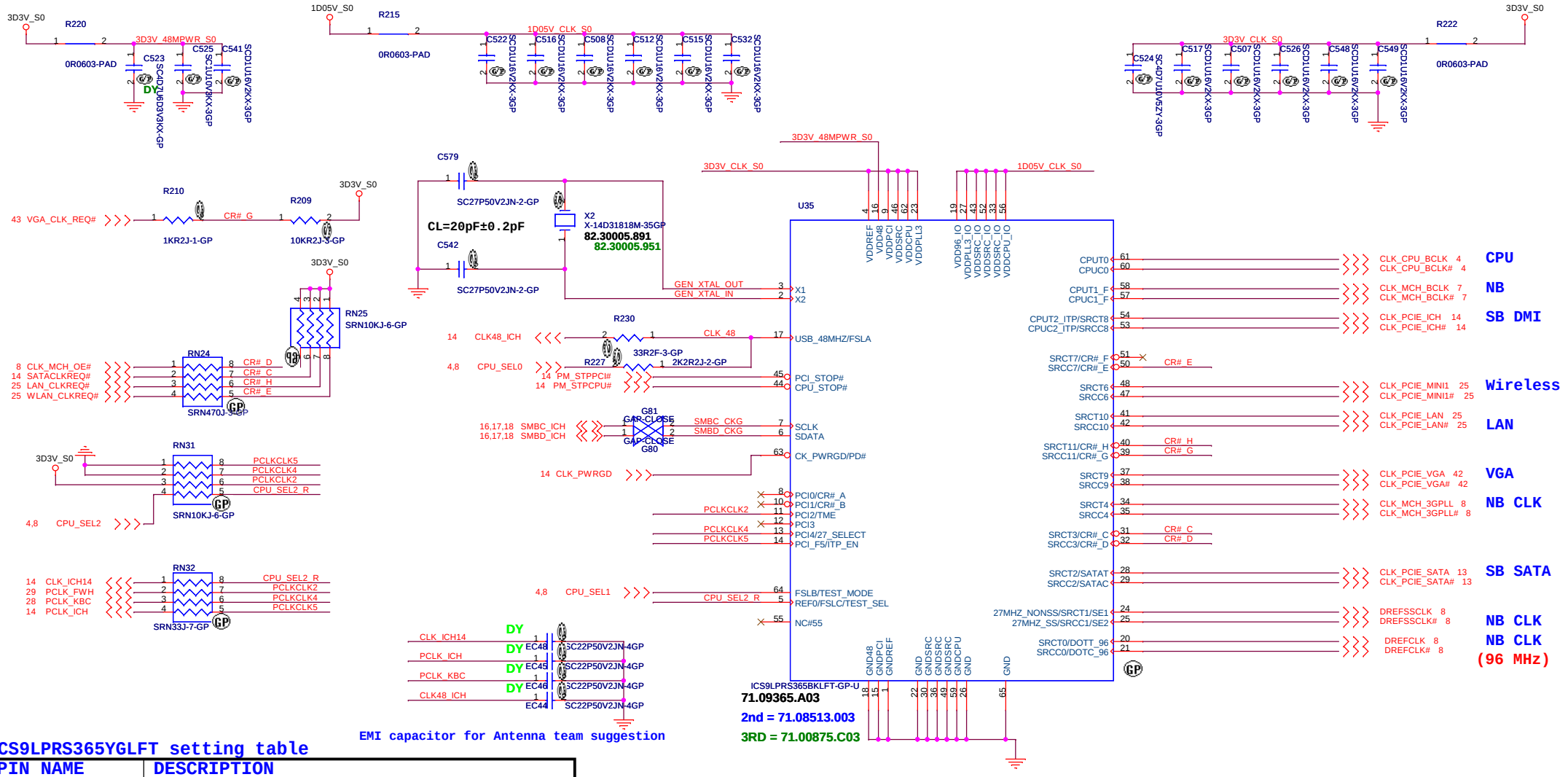
Title: ***Reference***

Size: A3 | Document Number: **JM41 Discrete** | Rev: -2

Date: Tuesday, April 28, 2009 | Sheet 2 of 48



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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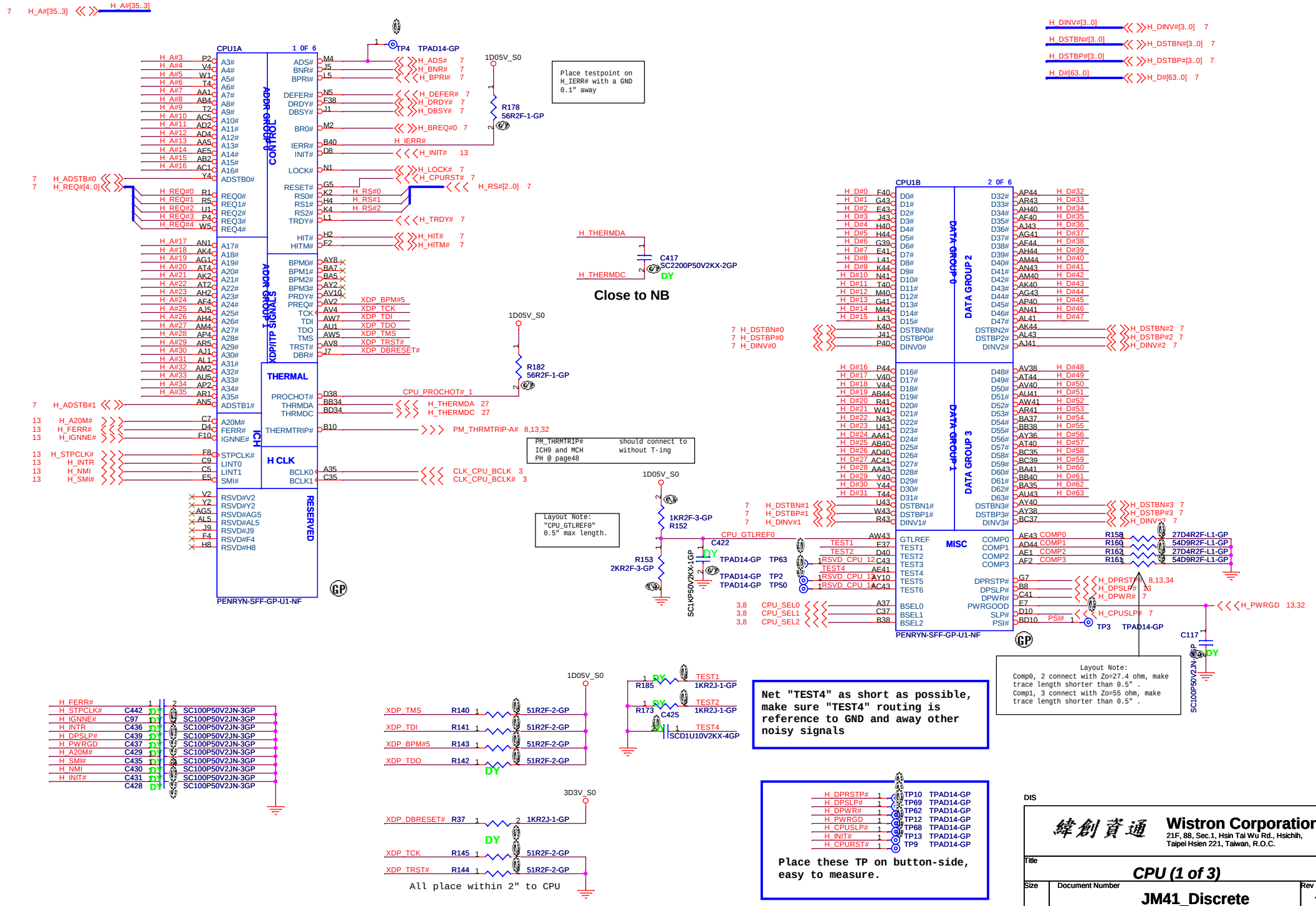
CPU1A
1 OF 6
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
ADDR GROUP 1
THERMAL
H CLK
RESERVED
PENRYN-SFF-GP-U1-NF
TP4 TPAD14-GP
1D05V_S0
R178 56R2F-1-GP
R182 56R2F-1-GP
Place testpoint on H_IERR# with a GND 0.1" away
H_THERMDA
H_THERMDC
C417 SC2200P50V2KX-2GP
DY
Close to NB
CPU_PROCHOT# 1
PM_THRMTRIP-A# 8,13,32
PM_THRMTRIP# should connect to ICH9 and MCH PH @ page48
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CPU1B
2 OF 6
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
PENRYN-SFF-GP-U1-NF
1KR2F-3-GP R152
R153 2KR2F-3-GP
SC1KP50V2KX-1GP
CPU_GTLREF0
C422
TPAD14-GP TP63
TPAD14-GP TP2
TPAD14-GP TP50
3,8 CPU_SEL0
3,8 CPU_SEL1
3,8 CPU_SEL2
Layout Note: "CPU_GTLREF0" 0.5" max length.
H_DINV#[3..0]
H_DSTBN#[3..0]
H_DSTBP#[3..0]
H_D#[63..0]
H_PWRGD 13,32
H_CPUSLP# 7
H_DPRSTP# 8,13,34
H_DPSLP# 13
H_DPWR# 7
TP3 TPAD14-GP
C117
SC100P50V2JN-3GP
DY
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
R158 27D4R2F-L1-GP
R160 54D9R2F-L1-GP
R162 27D4R2F-L1-GP
R161 54D9R2F-L1-GP
TEST1 1KR2J-1-GP
TEST2 1KR2J-1-GP
TEST4 SCD1U10V2KX-4GP
C425
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
XDP_TMS R140 51R2F-2-GP
XDP_TDI R141 51R2F-2-GP
XDP_BPM#5 R143 51R2F-2-GP
XDP_TDO R142 51R2F-2-GP
3D3V_S0
XDP_DBRESET# R37 1KR2J-1-GP
XDP_TCK R145 51R2F-2-GP
XDP_TRST# R144 51R2F-2-GP
All place within 2" to CPU
H_FERR# C442 SC100P50V2JN-3GP
H_STPCLK# C97 SC100P50V2JN-3GP
H_IGNNE# C436 SC100P50V2JN-3GP
H_INTR C439 SC100P50V2JN-3GP
H_DPSLP# C437 SC100P50V2JN-3GP
H_PWRGD C429 SC100P50V2JN-3GP
H_A20M# C435 SC100P50V2JN-3GP
H_SMI# C430 SC100P50V2JN-3GP
H_NMI C431 SC100P50V2JN-3GP
H_INIT# C428 SC100P50V2JN-3GP
H_DPRSTP# TP10 TPAD14-GP
H_DPSLP# TP69 TPAD14-GP
H_DPWR# TP62 TPAD14-GP
H_PWRGD TP12 TPAD14-GP
H_CPUSLP# TP68 TPAD14-GP
H_INIT# TP13 TPAD14-GP
H_CPURST# TP9 TPAD14-GP
Place these TP on button-side, easy to measure.
DIS
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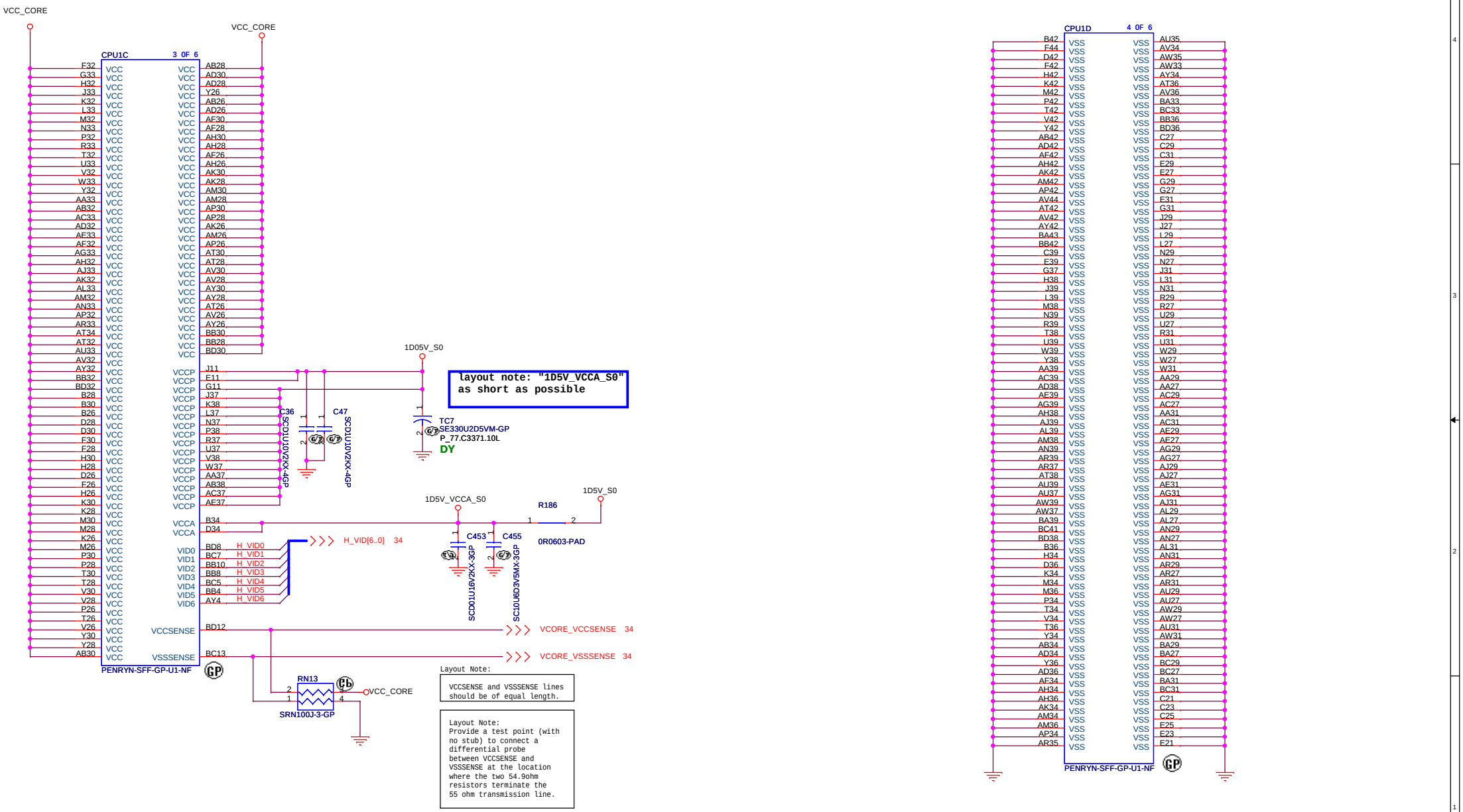
Title
CPU (1 of 3)
Size
Document Number
JM41_Discrete
Rev
-2
Date: Tuesday, May 05, 2009
Sheet 4 of 48



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Title	CPU (2 of 3)
Size	
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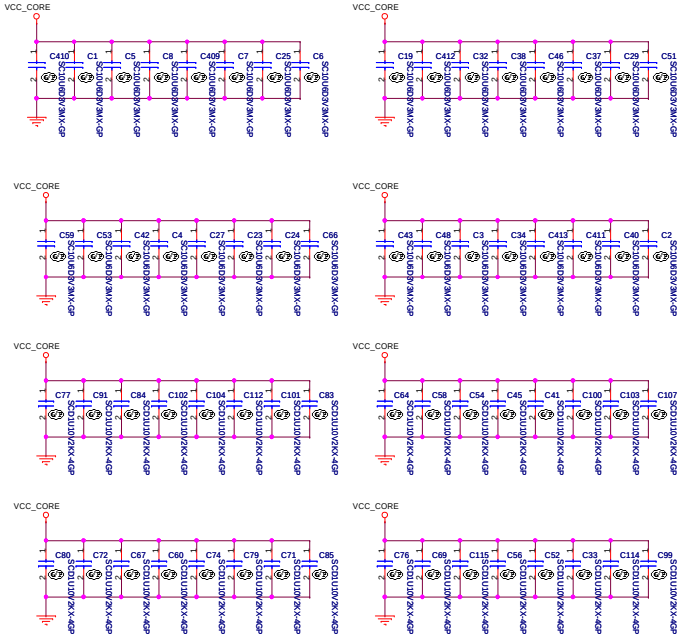
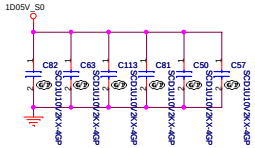
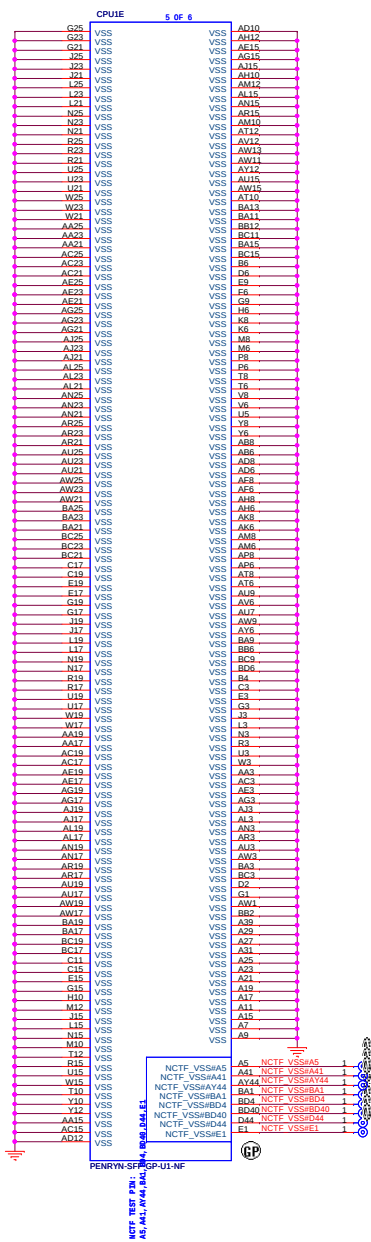
Place these inside socket
cavity on L8(North side Secondary)



Place these inside socket
cavity on L8(North side Secondary)





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Title	CPU (3 of 3)		
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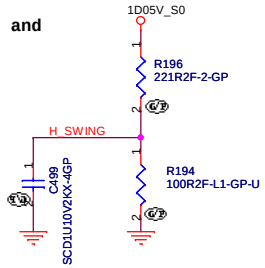
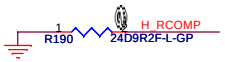
H_SWING routing Trace width and Spacing use 10 / 20 mil

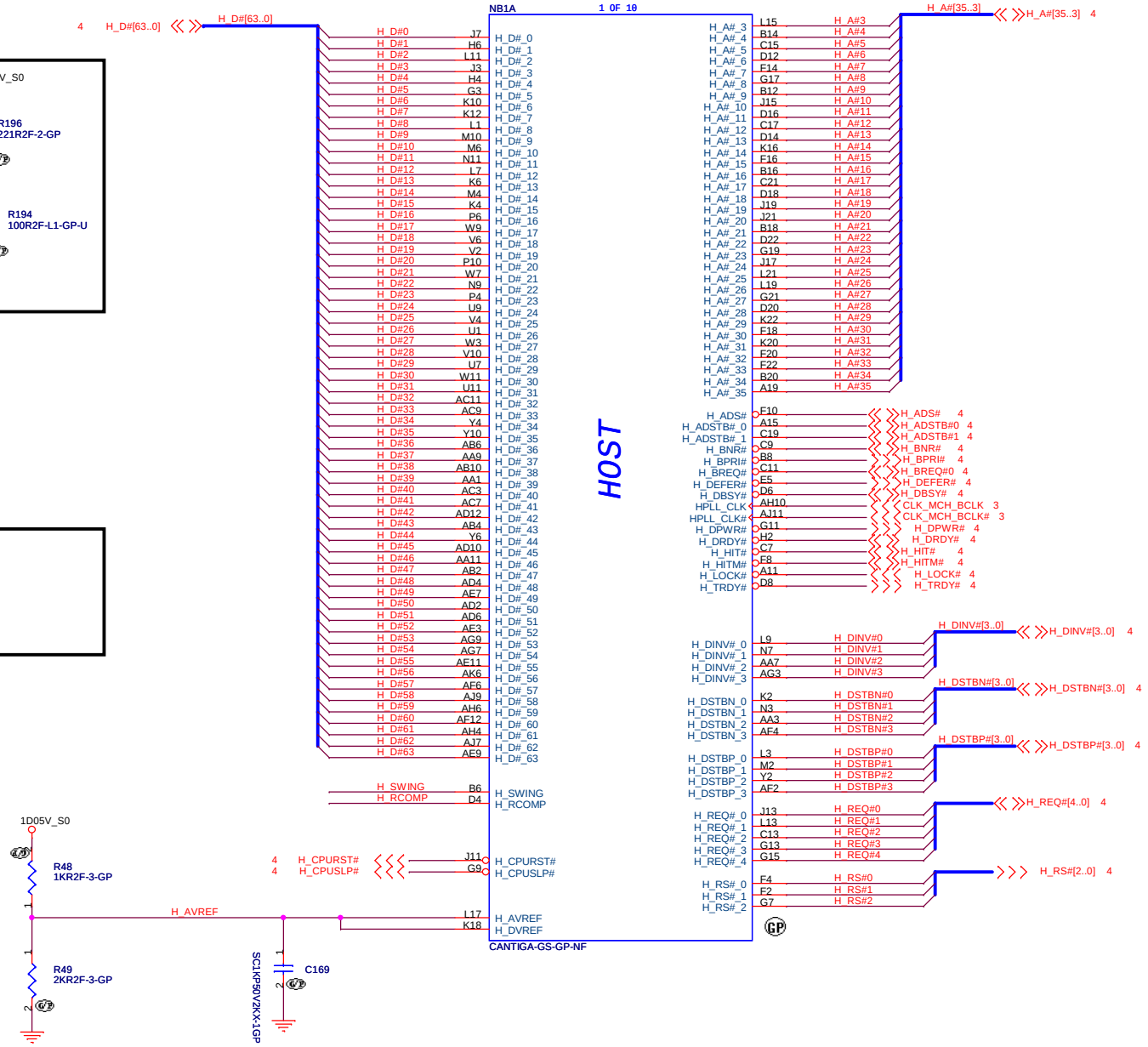
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



DIS

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Title	***Cantiga (1 of 6)***	
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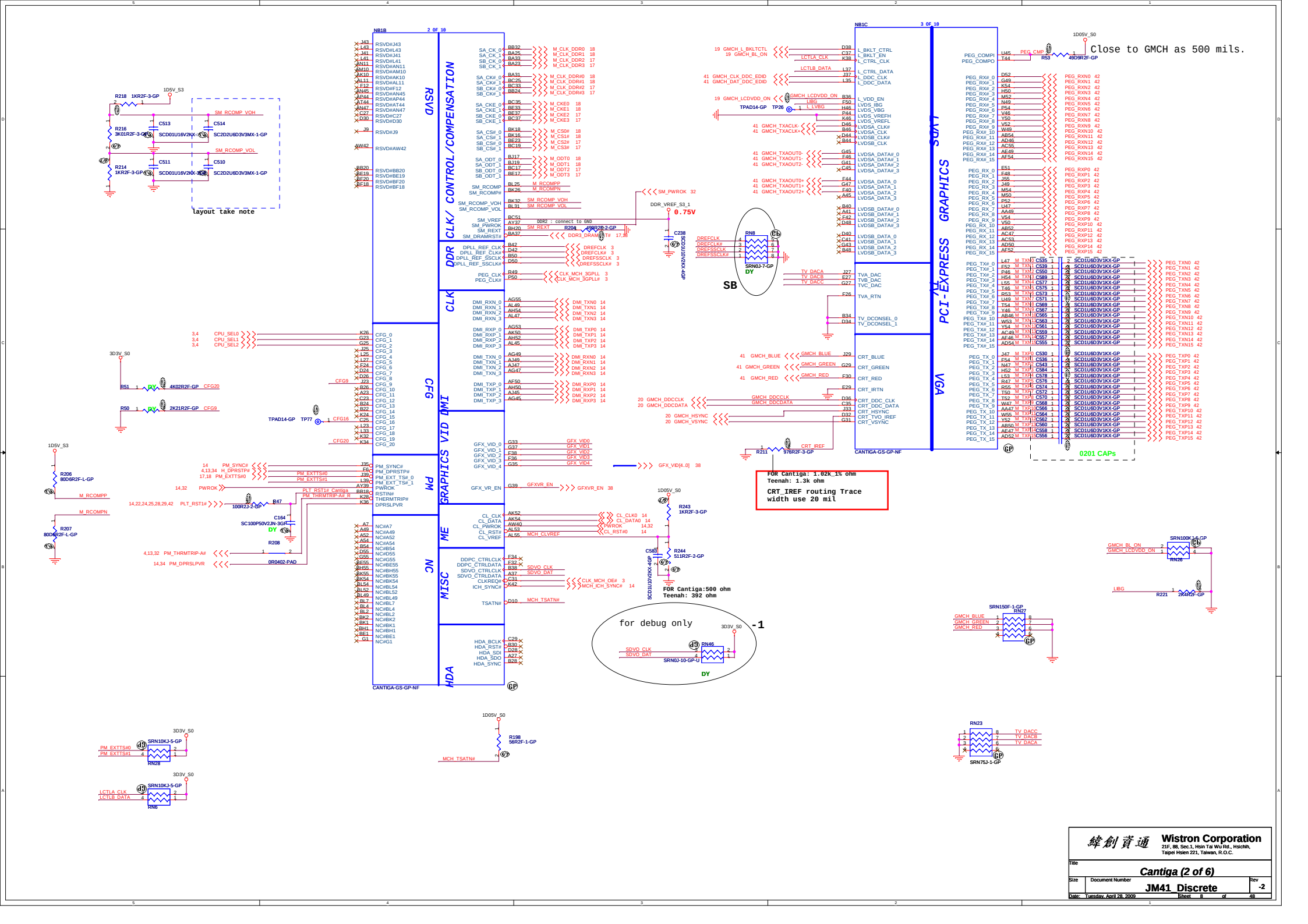
Close to GMCH as 500 mils.
layout take note
SB
for debug only
-1
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
0201 CAPs
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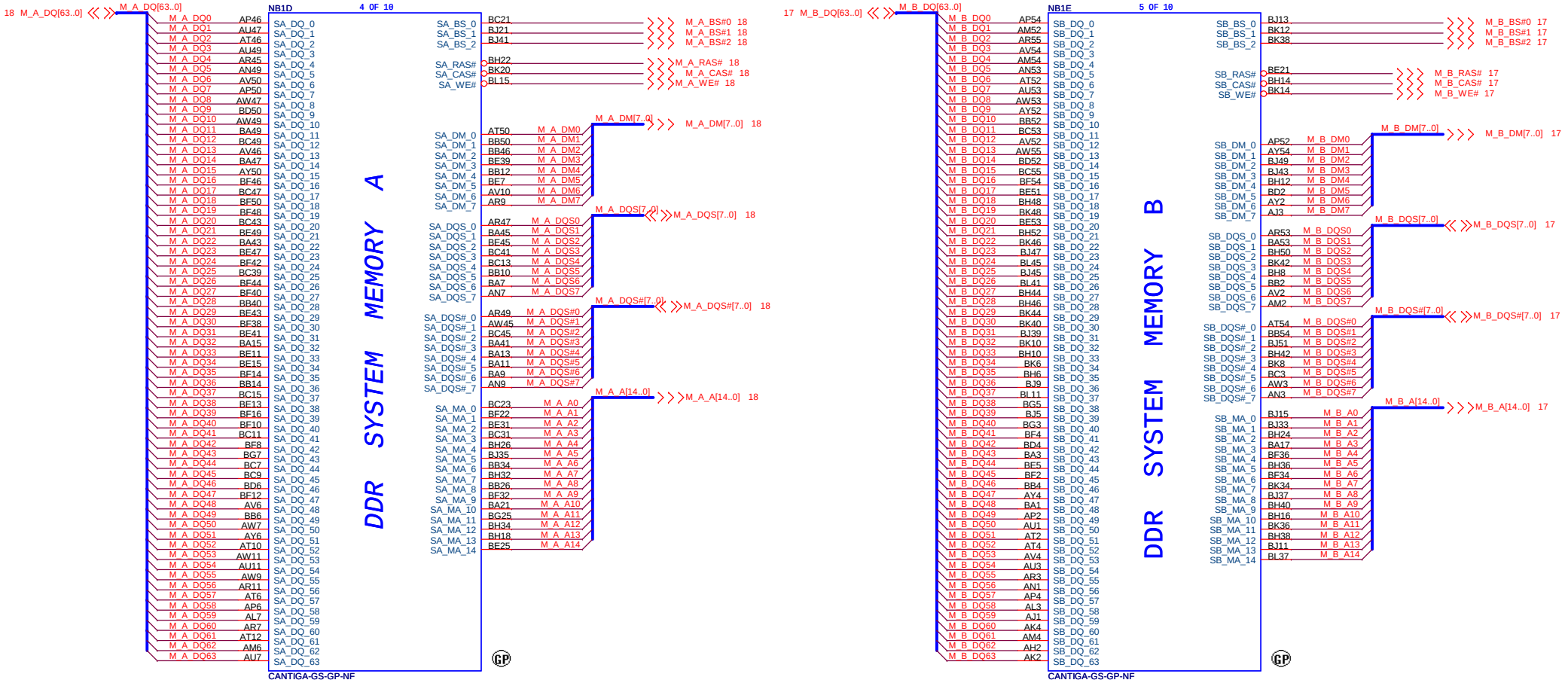
Cantiga (2 of 6)
JM41_Discrete
-2
Tuesday, April 28, 2009



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Title: ***Cantiga (3 of 6)***

Size	Document Number	Rev
	JM41_Discrete	-2

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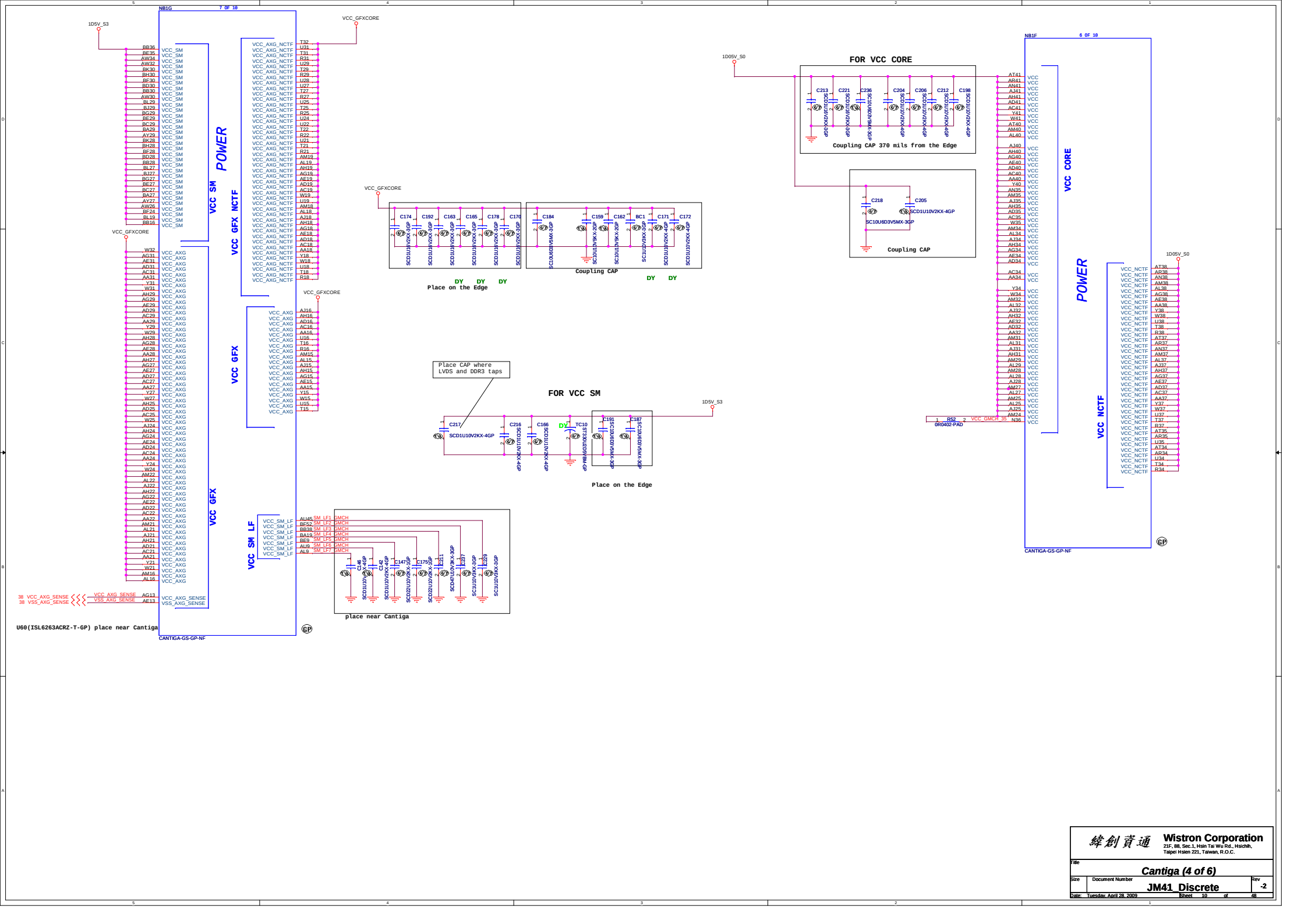

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Title: Cantiga (4 of 6)		
Size	Document Number: JM41_Discrete	Rev: -2
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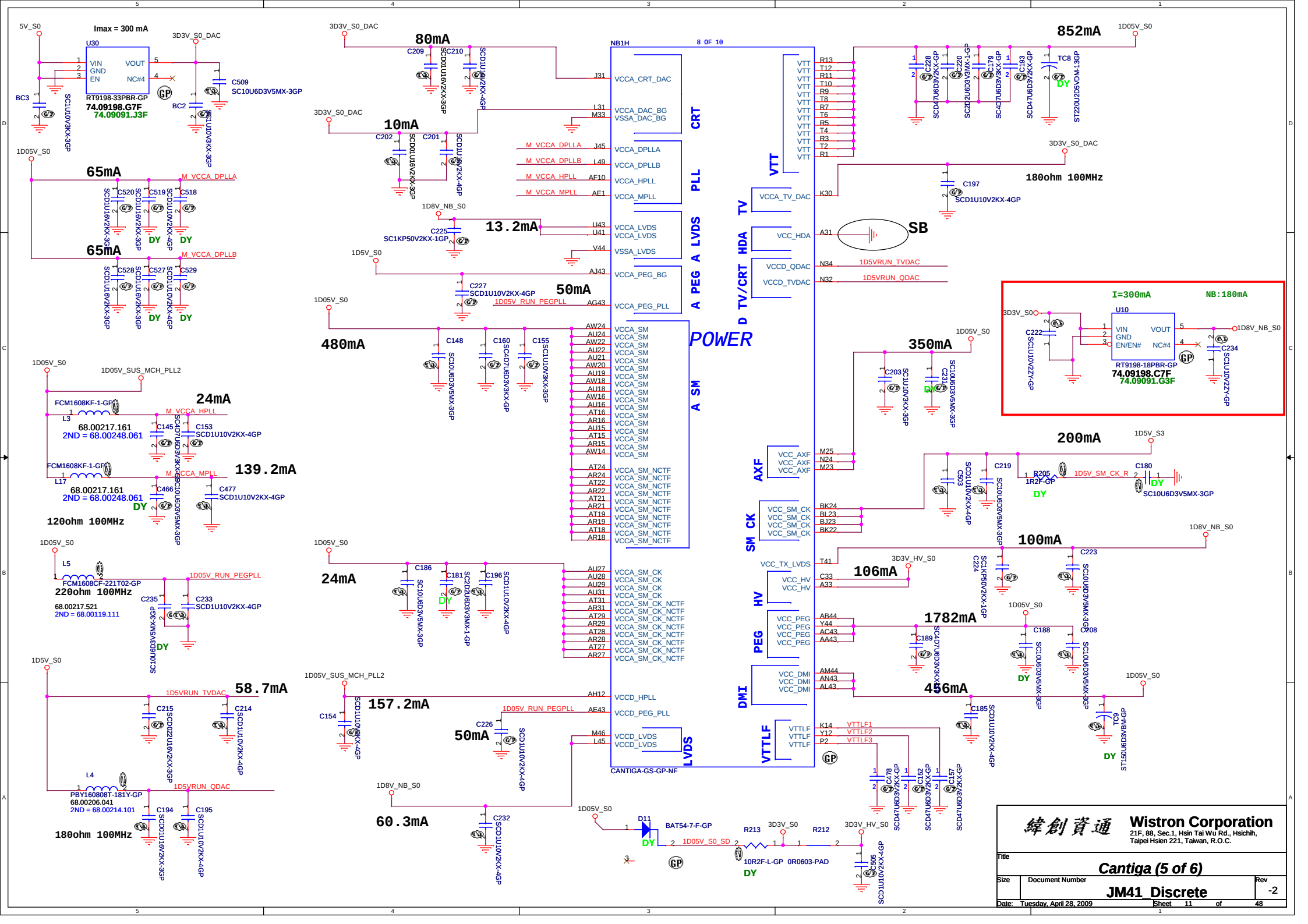

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Title	***Cantiga (5 of 6)***
Size	Document Number: **JM41_Discrete**
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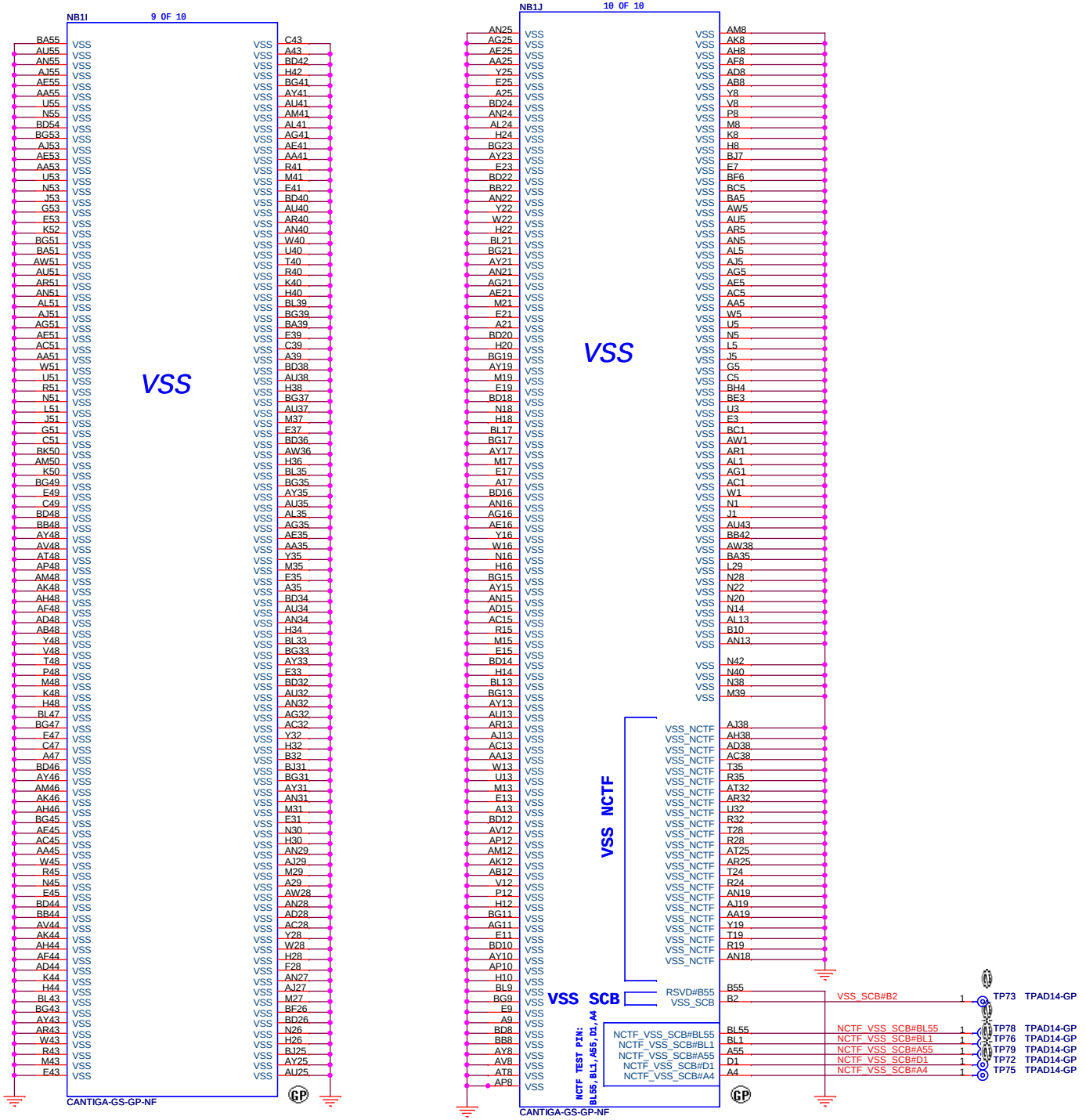
Date: Tuesday, April 28, 2009	Sheet 11 of 48



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Title: ***Cantiga (6 of 6)***

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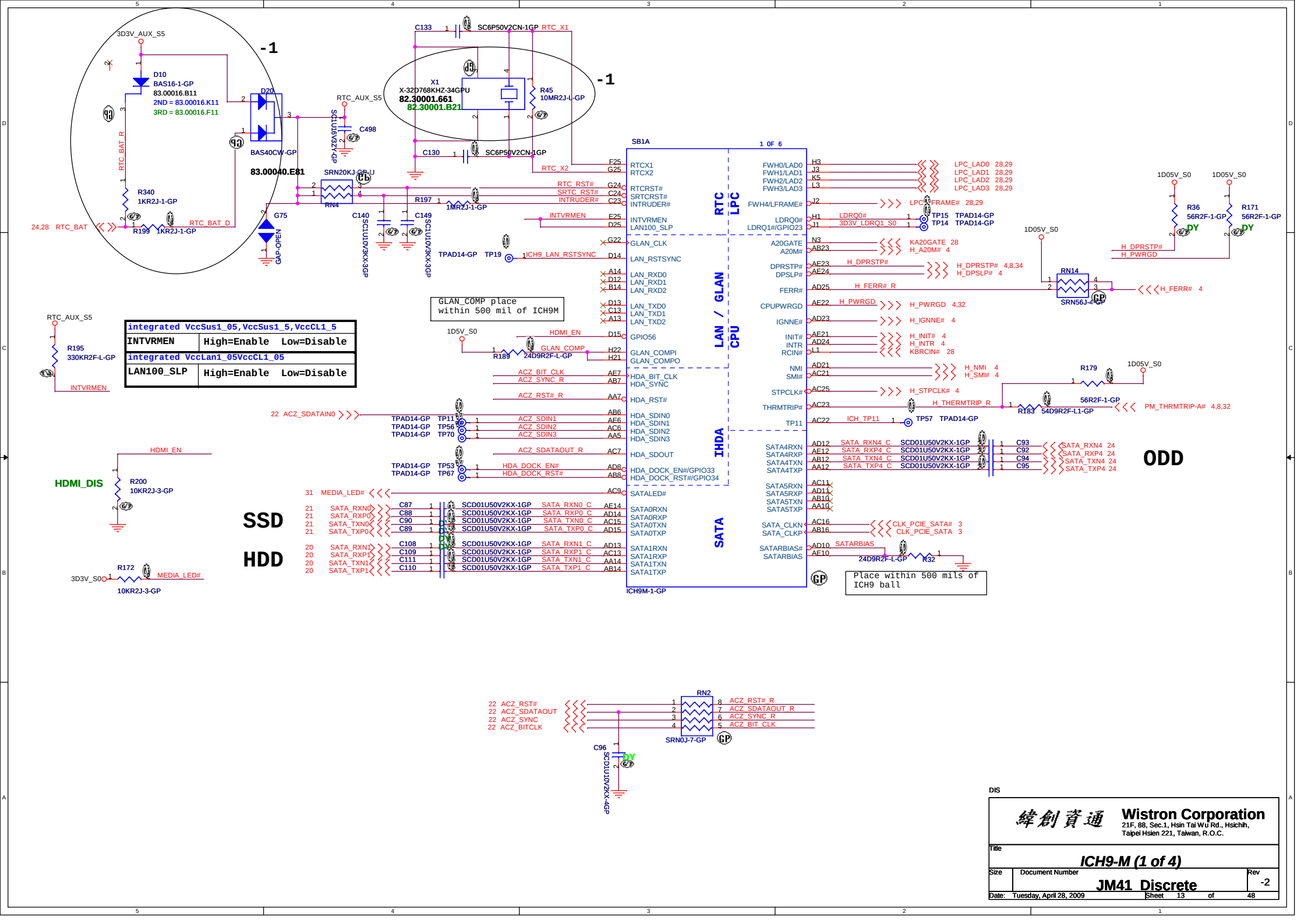
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
SSD
HDD
ODD
SB1A
ICH9M-1-GP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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ICH9-M (1 of 4)
JM41 Discrete
Tuesday, April 28, 2009

PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

CHANGE to GPO28(original is GPIO18)

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	WiMAX
4	WEBCAM
5	NC
6	NC
7	BLUETOOTH
8	NC
9	USB1
10	MINIC2
11	Cardreader

These R need close SB within 600 mils

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Title: ICH9-M (2 of 4)

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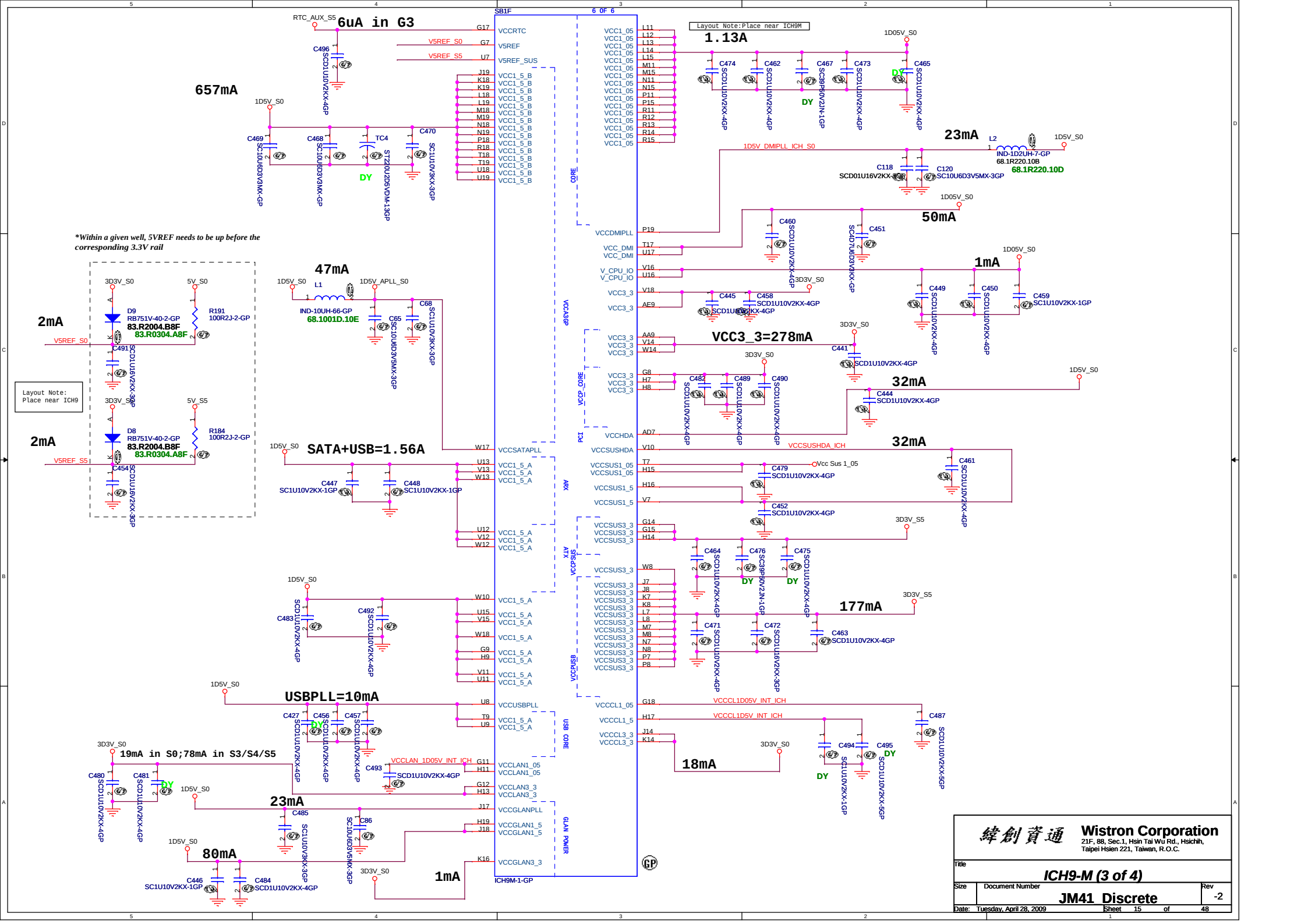
6uA in G3
657mA
1.13A
23mA
50mA
1mA
2mA
2mA
47mA
VCC3_3=278mA
32mA
32mA
SATA+USB=1.56A
USBPLL=10mA
19mA in S0;78mA in S3/S4/S5
177mA
23mA
80mA
1mA
18mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
SB1F
6 OF 6
ICH9M-1-GP
Wistron Corporation
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ICH9-M (3 of 4)
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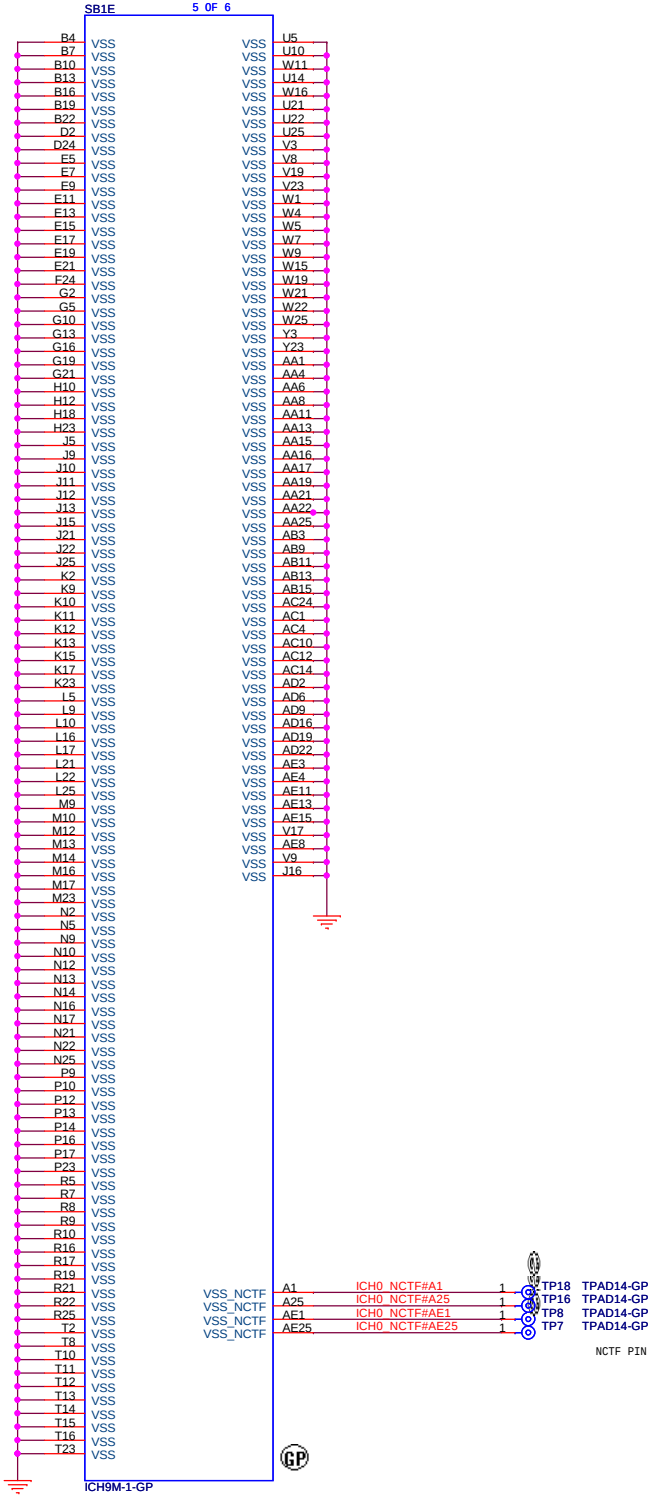
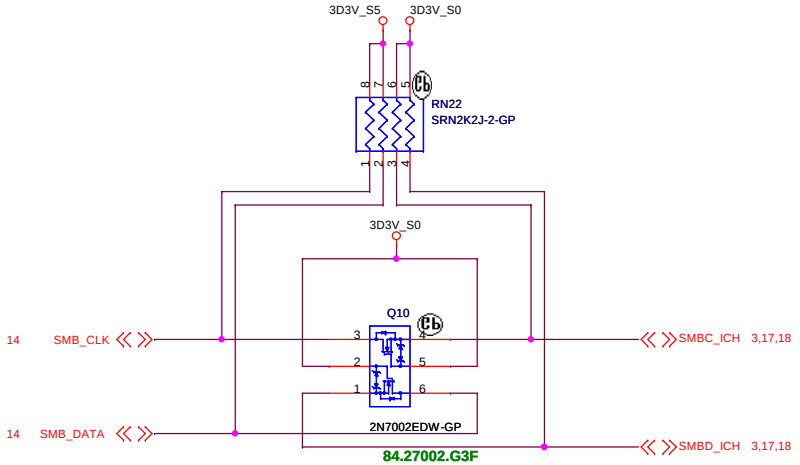
48





SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (4 of 4)*

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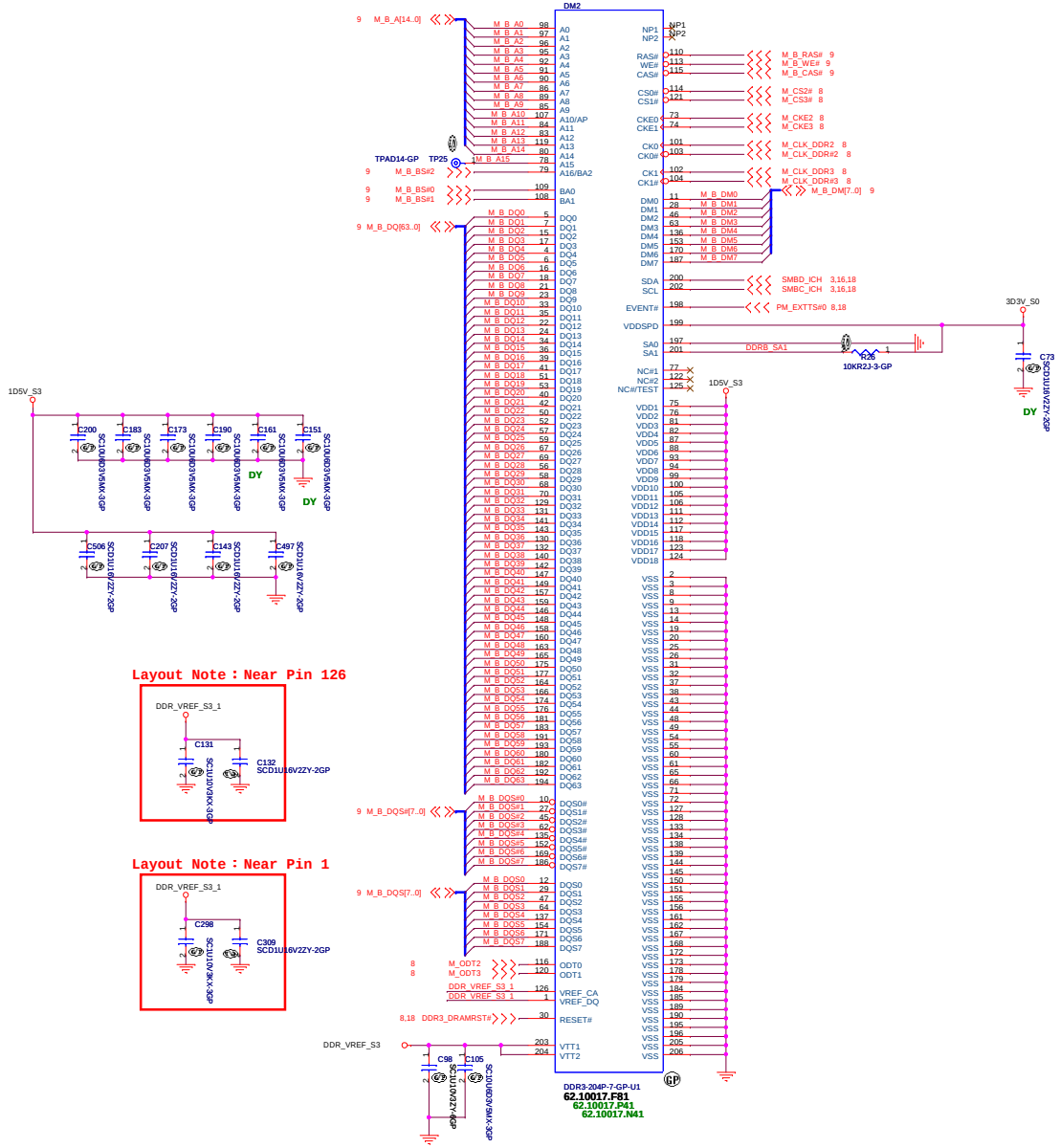
DDR3 SOCKET_1



緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	DDR3 Socket1		
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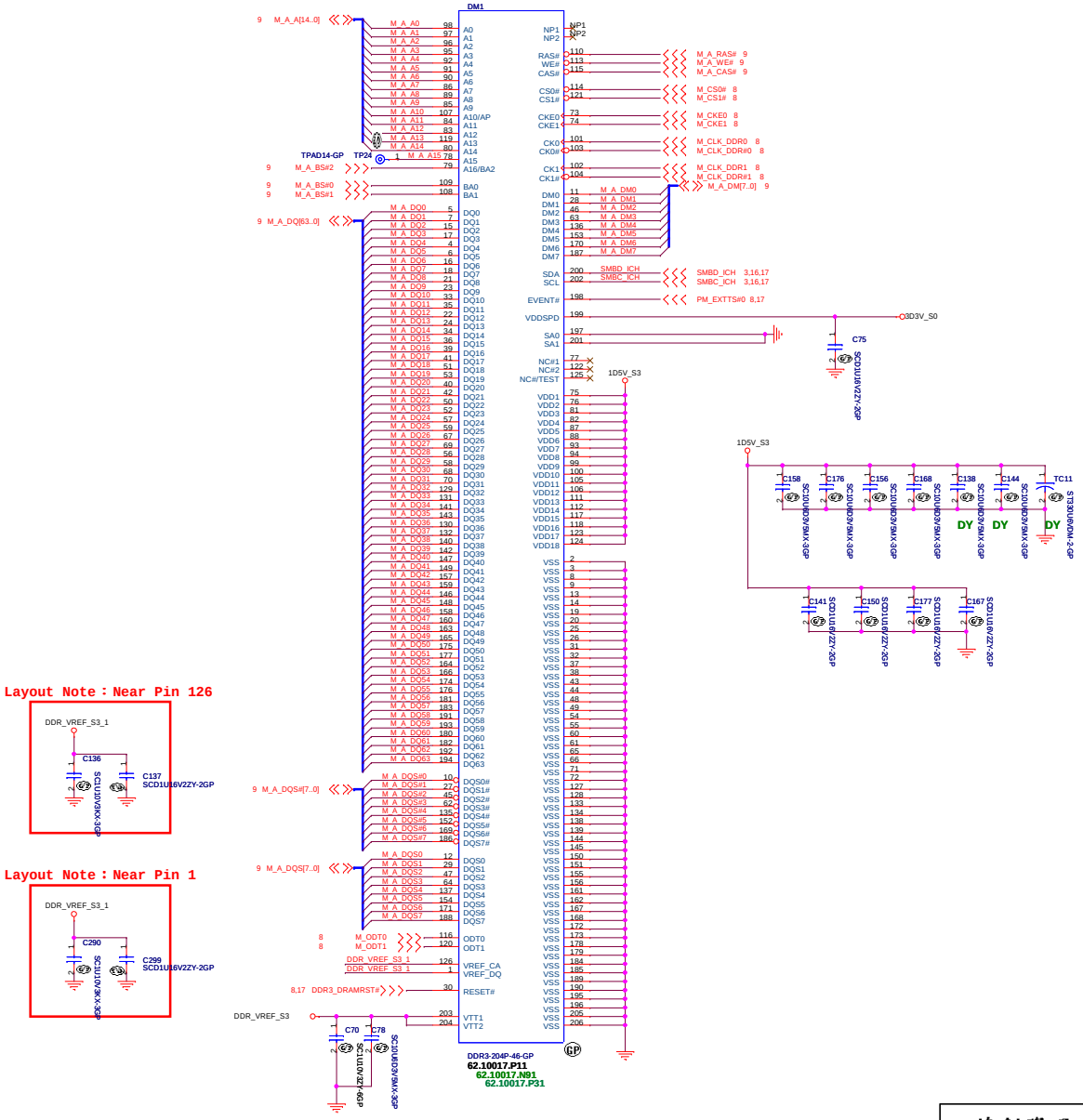
Date: Tuesday, April 28, 2009	Sheet 17 of 48		

DDR3 SOCKET_2



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Title	DDR3 Socket2		
Size	Document Number	JM41_Discrete	Rev -2
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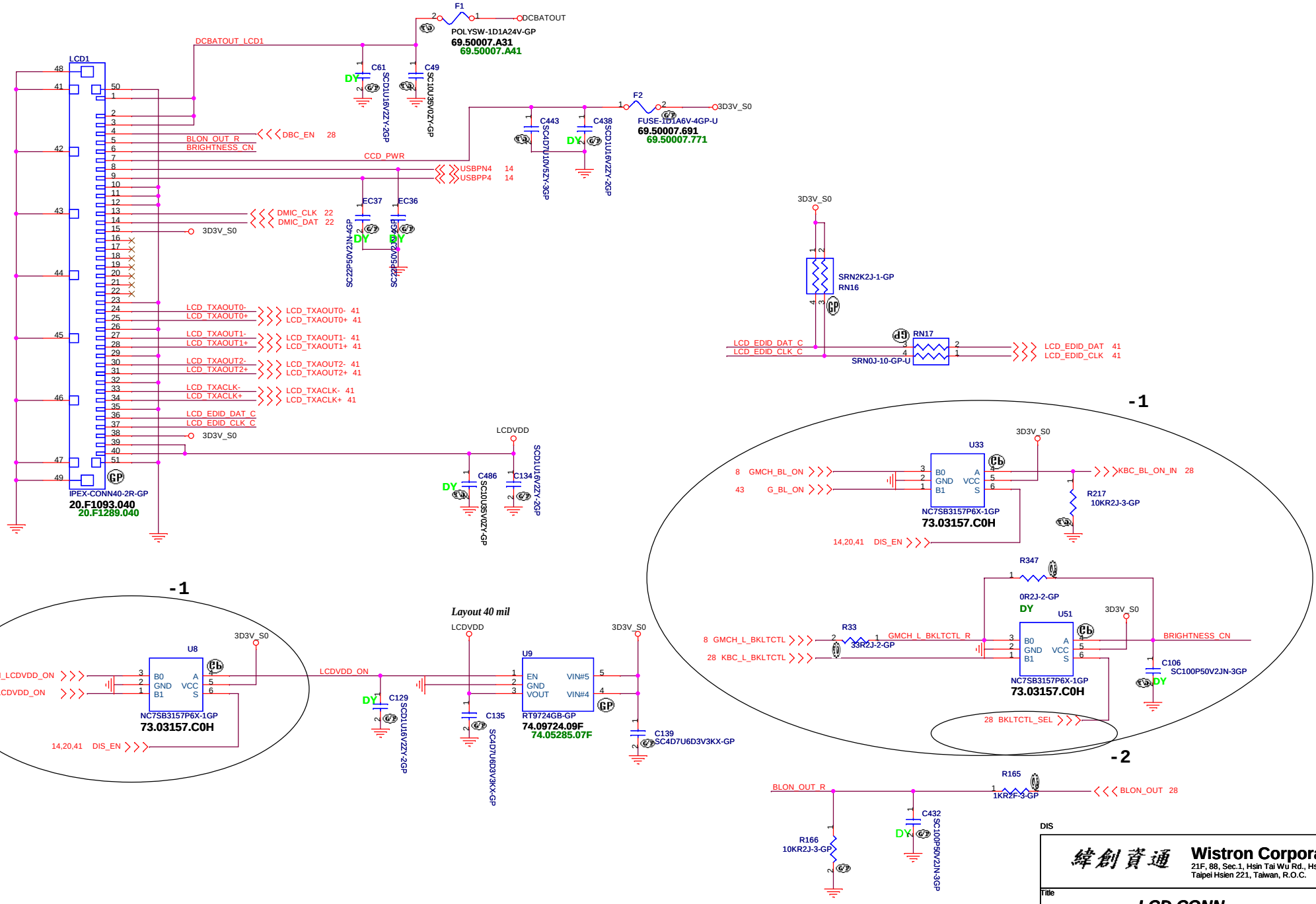
LCD/CCD CONN

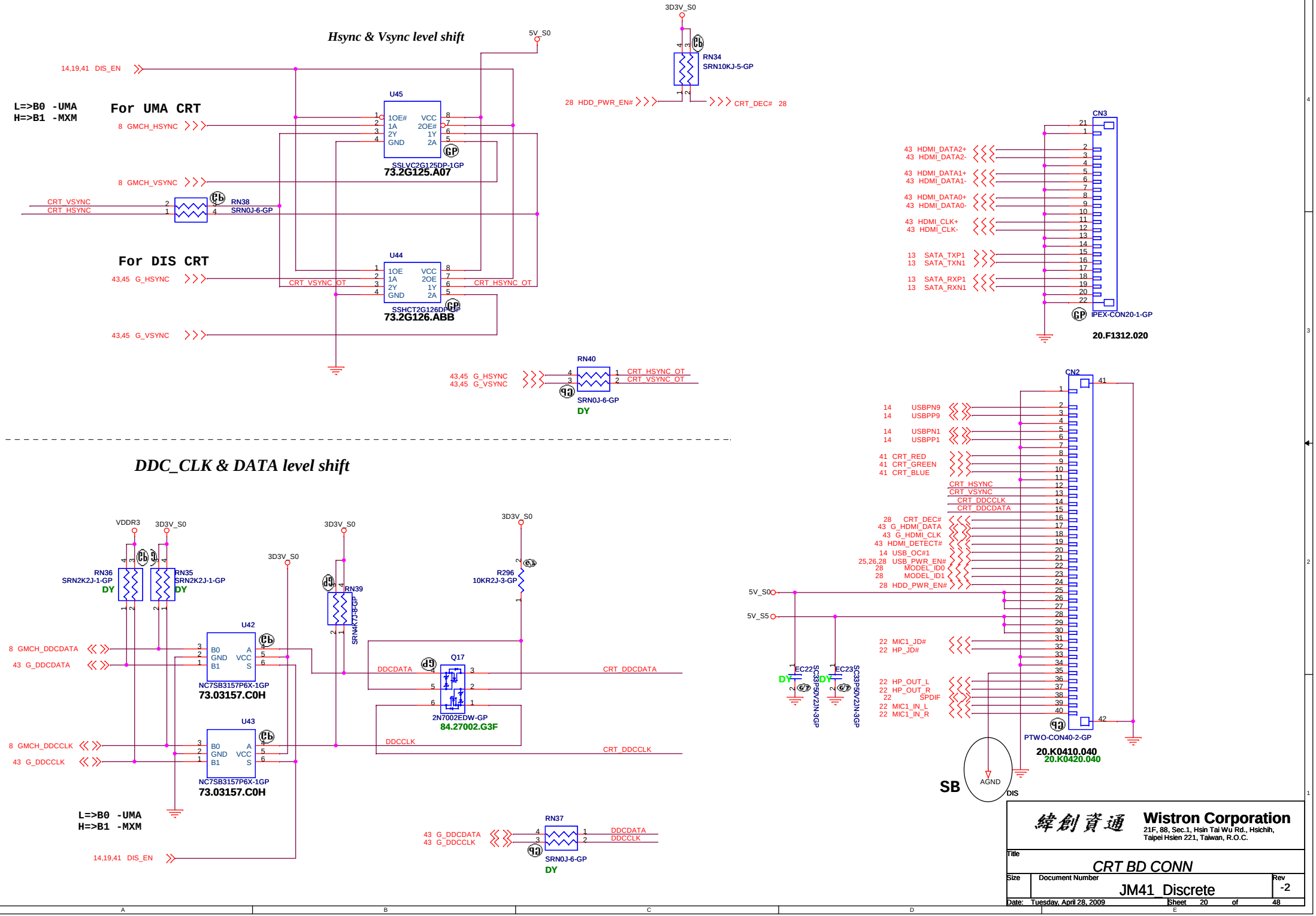
Internal MIC



DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size	Document Number: JM41_Discrete	Rev: -2
Date: Tuesday, April 28, 2009	Sheet 19 of 48	


Hsync & Vsync level shift
L=>B0 -UMA
H=>B1 -MXM
For UMA CRT
For DIS CRT
14,19,41 DIS_EN
8 GMCH_HSYNC
8 GMCH_VSYNC
CRT_VSYNC
CRT_HSYNC
RN38
SRN0J-6-GP
U45
SSLVC2G125DP-1GP
73.2G125.A07
U44
SSHCT2G126DP-1GP
73.2G126.ABB
43,45 G_HSYNC
43,45 G_VSYNC
CRT_VSYNC_OT
CRT_HSYNC_OT
5V_S0
3D3V_S0
RN34
SRN10KJ-5-GP
28 HDD_PWR_EN#
CRT_DEC# 28
RN40
SRN0J-6-GP
DY
CN3
IPEX-CON20-1-GP
20.F1312.020
43 HDMI_DATA2+
43 HDMI_DATA2-
43 HDMI_DATA1+
43 HDMI_DATA1-
43 HDMI_DATA0+
43 HDMI_DATA0-
43 HDMI_CLK+
43 HDMI_CLK-
13 SATA_TXP1
13 SATA_TXN1
13 SATA_RXP1
13 SATA_RXN1
DDC_CLK & DATA level shift
VDDR3
RN36
SRN2K2J-1-GP
RN35
SRN2K2J-1-GP
RN39
SRN4K7J-8-GP
R296
10KR2J-3-GP
U42
U43
NC7SB3157P6X-1GP
73.03157.C0H
Q17
2N7002EDW-GP
84.27002.G3F
8 GMCH_DDCDATA
43 G_DDCDATA
8 GMCH_DDCCLK
43 G_DDCCLK
DDCDATA
DDCCLK
CRT_DDCDATA
CRT_DDCCLK
RN37
SRN0J-6-GP
CN2
PTWO-CON40-2-GP
20.K0410.040
20.K0420.040
14 USBPN9
14 USBPP9
14 USBPN1
14 USBPP1
41 CRT_RED
41 CRT_GREEN
41 CRT_BLUE
CRT_HSYNC
CRT_VSYNC
CRT_DDCCLK
CRT_DDCDATA
28 CRT_DEC#
43 G_HDMI_DATA
43 G_HDMI_CLK
43 HDMI_DETECT#
14 USB_OC#1
25,26,28 USB_PWR_EN#
28 MODEL_ID0
28 MODEL_ID1
28 HDD_PWR_EN#
5V_S0
5V_S5
EC22
EC23
SC33P50V2JN-3GP
22 MIC1_JD#
22 HP_JD#
22 HP_OUT_L
22 HP_OUT_R
22 SPDIF
22 MIC1_IN_L
22 MIC1_IN_R
SB
AGND
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT BD CONN
Size
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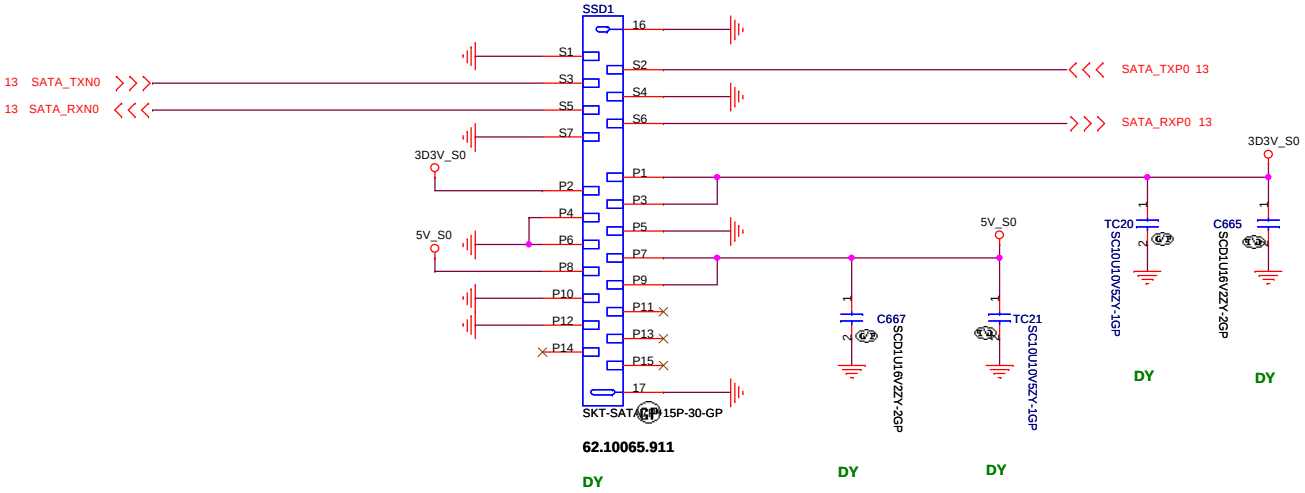
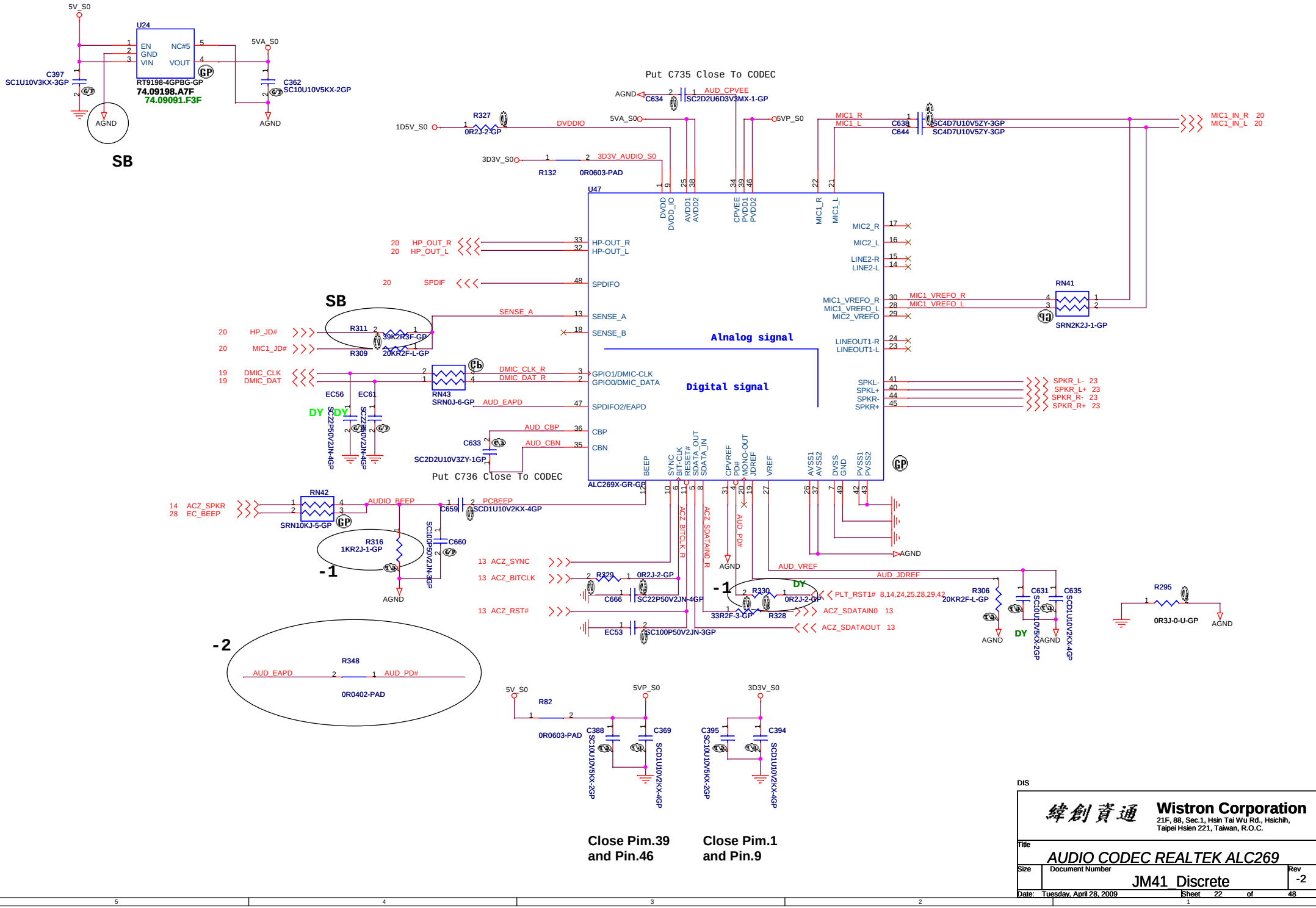
SSD SATA Connector



DIS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *HDD CONN*		
Size	Document Number: JM41 Discrete	Rev: -2
Date: Tuesday, April 28, 2009	Sheet 21 of 48	


5V_S0
U24
EN
GND
VIN
NC#5
VOUT
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
5VA_S0
C397
SC1U10V3KX-3GP
C362
SC10U10V5KX-2GP
AGND
SB
Put C735 Close To CODEC
AUD_CPVEE
SC2D2U6D3V3MX-1-GP
1D5V_S0
R327
0R2J-2-GP
DVDDIO
3D3V_S0
R132
0R0603-PAD
3D3V_AUDIO_S0
MIC1_R
MIC1_L
SC4D7U10V5ZY-3GP
MIC1_IN_R 20
MIC1_IN_L 20
U47
DVDD
DVDD_IO
AVDD1
AVDD2
CPVEE
PVDD1
PVDD2
HP-OUT-R
HP-OUT-L
SPDIFO
SENSE_A
SENSE_B
GPIO1/DMIC-CLK
GPIO0/DMIC_DATA
SPDIFO2/EAPD
CBP
CBN
MIC2_R
MIC2_L
LINE2-R
LINE2-L
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
LINEOUT1-R
LINEOUT1-L
SPKL-
SPKL+
SPKR-
SPKR+
20 HP_OUT_R
20 HP_OUT_L
20 SPDIFO
20 HP_JD#
20 MIC1_JD#
19 DMIC_CLK
19 DMIC_DAT
R311
39K2R3F-GP
R309
20KR2F-L-GP
RN43
SRN0J-6-GP
DMIC_CLK_R
DMIC_DAT_R
AUD_EAPD
AUD_CBP
AUD_CBN
C633
SC2D2U10V3ZY-1GP
EC56
EC61
SC22P50V2JN-4GP
DY
Put C736 Close To CODEC
Alnalog signal
Digital signal
ALC269X-GR-GP
BEEP
SYNC
BIT-CLK
RESET#
SDATA_OUT
SDATA_IN
CPVREF
PD#
MONO-OUT
JDREF
VREF
AVSS1
AVSS2
DVSS
GND
PVSS1
PVSS2
RN41
SRN2K2J-1-GP
MIC1_VREFO_R
MIC1_VREFO_L
SPKR_L- 23
SPKR_L+ 23
SPKR_R- 23
SPKR_R+ 23
RN42
SRN10KJ-5-GP
14 ACZ_SPKR
28 EC_BEEP
AUDIO_BEEP
PCBEEP
SCD1U10V2KX-4GP
R316
1KR2J-1-GP
SC100P50V2JN-3GP
C660
C659
-1
13 ACZ_SYNC
13 ACZ_BITCLK
13 ACZ_RST#
ACZ_BITCLK_R
ACZ_SDATAIN0_R
AUD_PD#
R329
0R2J-2-GP
C666
SC22P50V2JN-4GP
EC53
SC100P50V2JN-3GP
R330
0R2J-2-GP
33R2F-3-GP
R328
PLT_RST1# 8,14,24,25,28,29,42
ACZ_SDATAIN0 13
ACZ_SDATAOUT 13
AUD_VREF
AUD_JDREF
R306
20KR2F-L-GP
C631
C635
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
R295
0R3J-0-U-GP
-2
R348
AUD_EAPD
AUD_PD#
0R0402-PAD
R82
0R0603-PAD
C388
C369
C395
C394
5VP_S0
3D3V_S0
Close Pim.39
and Pin.46
Close Pim.1
and Pin.9
DIS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC REALTEK ALC269
Size
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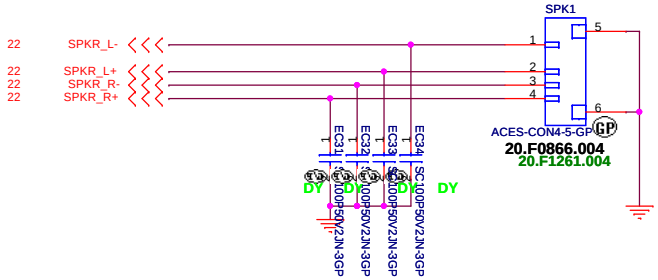
Internal Speaker



DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO JACK*	
Size	Document Number: JM41_Discrete	Rev: -2
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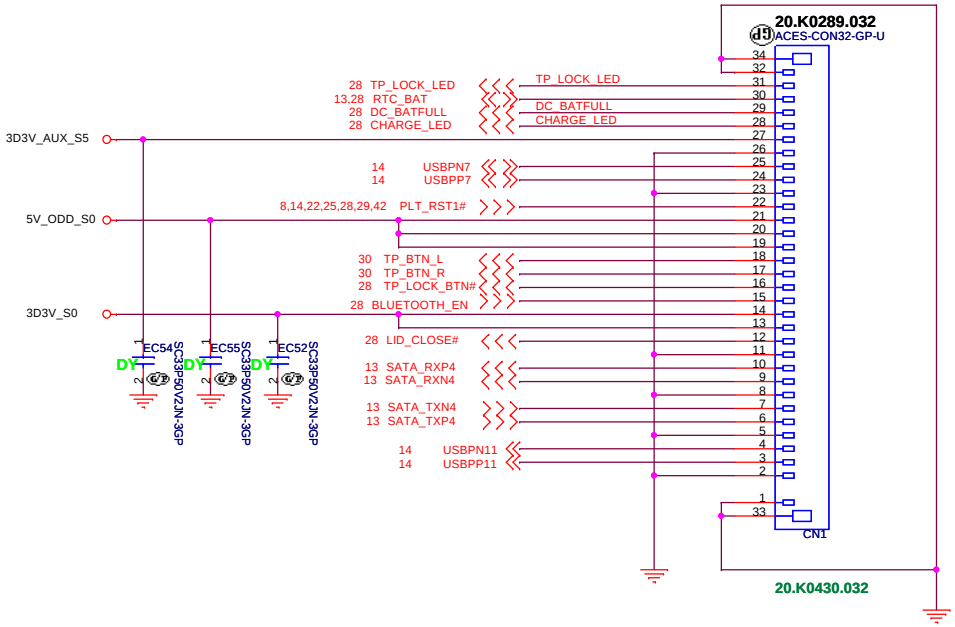


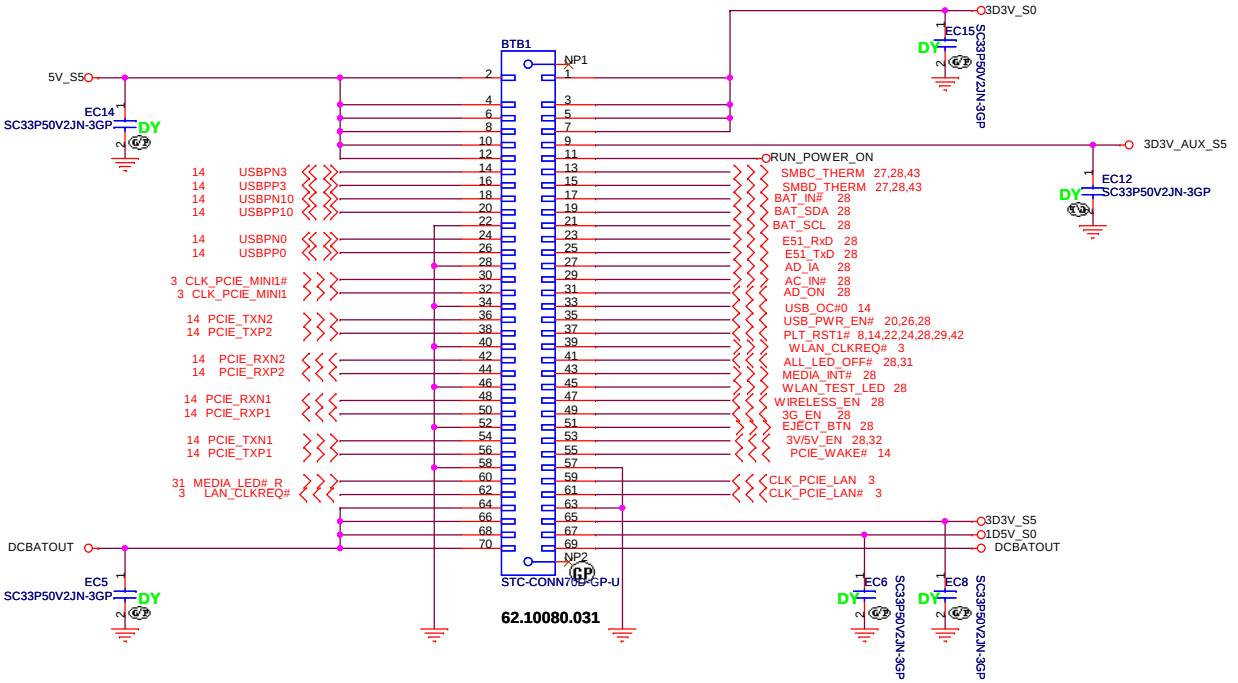
DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER BD CONN

Size	Document Number	Rev
	JM41_Discrete	-2

Date: Tuesday, April 28, 2009 Sheet 24 of 48



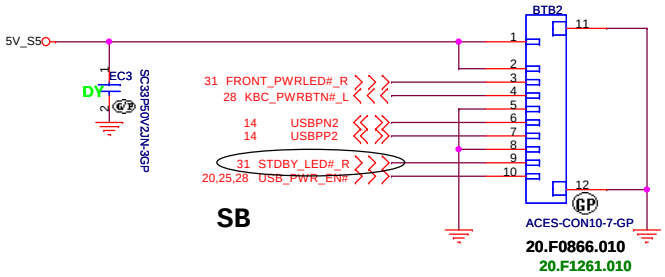
DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINI BD CONN***

Size	Document Number	Rev
A3	JM41_Discrete	-2

Date: Tuesday, April 28, 2009 Sheet 25 of 48



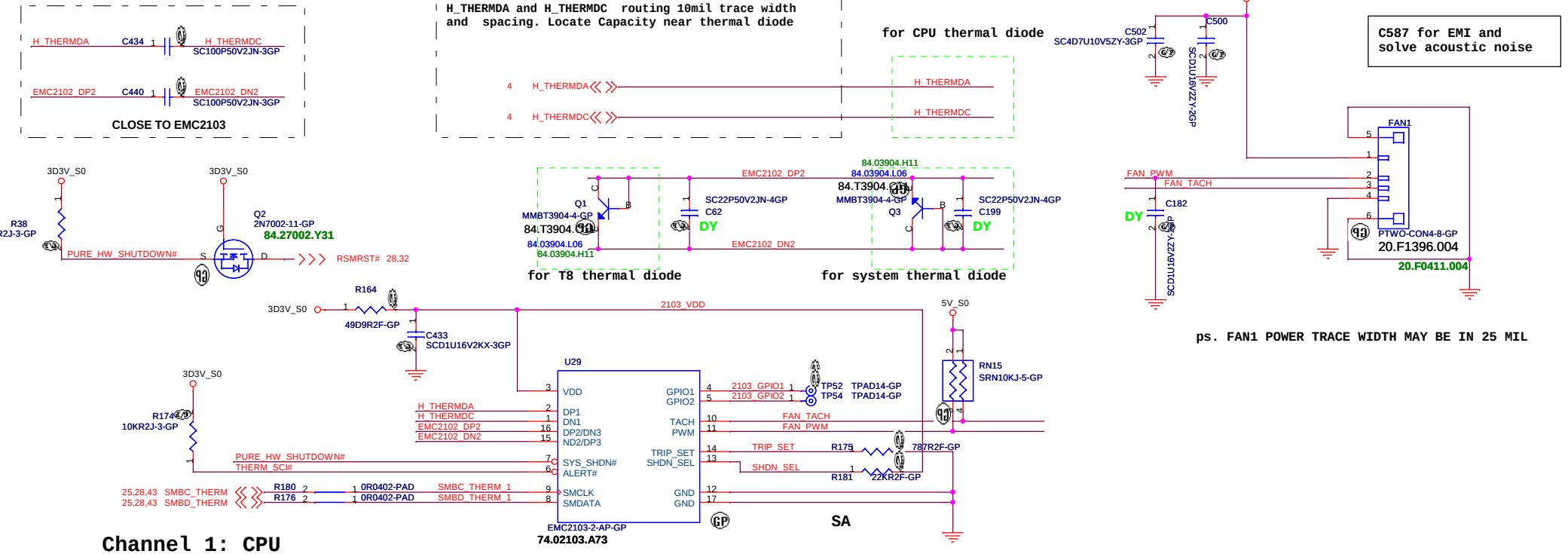
DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER BUTTON CONN**

Size	Document Number	Rev
A3	JM41_Discrete	-2

Date: Tuesday, April 28, 2009 Sheet 26 of 48



Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

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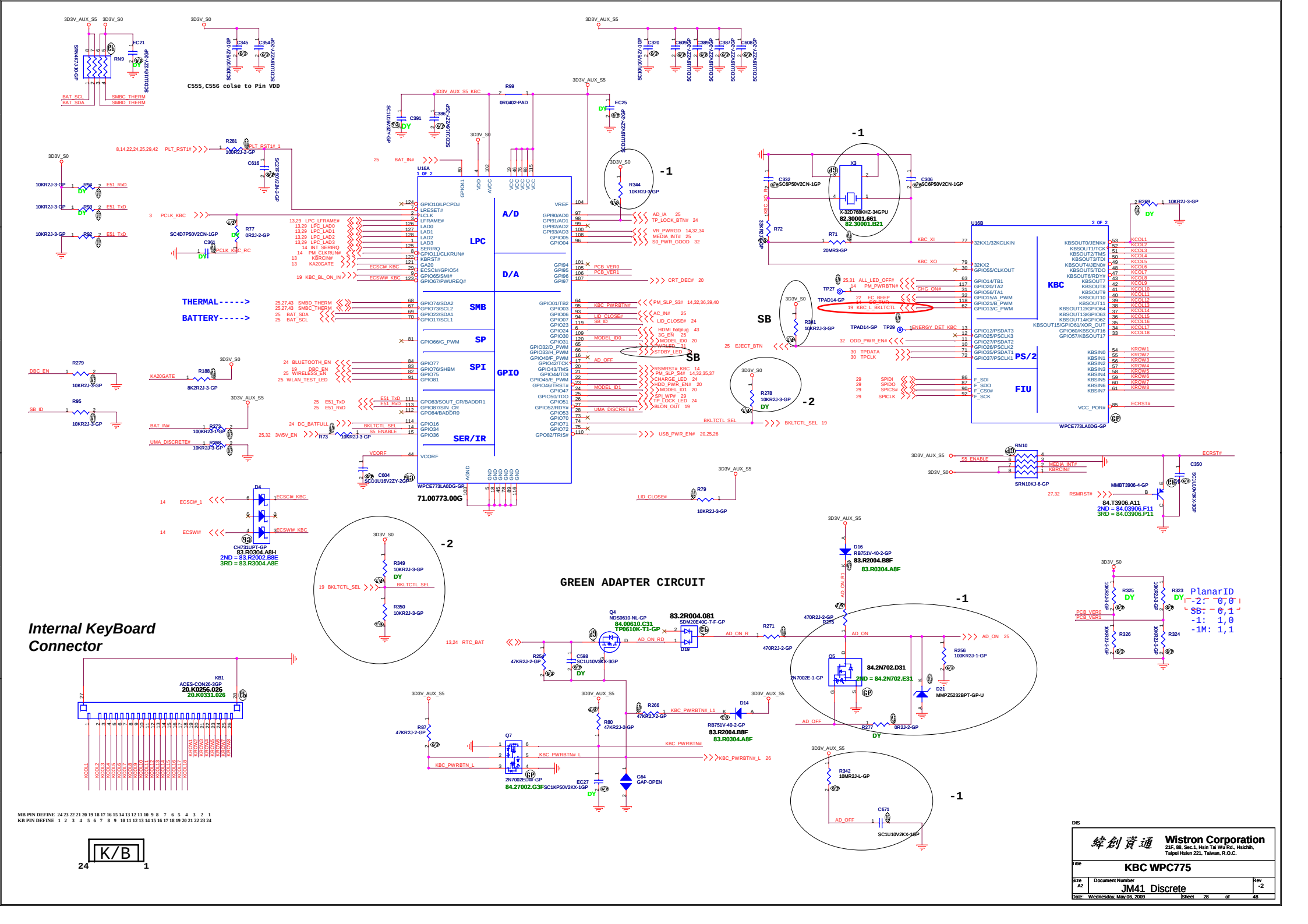
Internal KeyBoard Connector
KB1
ACES-CON26-3GP
20.K0256.026
20.K0331.026
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
24 1
C555,C556 colse to Pin VDD
THERMAL----->
BATTERY----->
U16A
1 OF 2
WPCE773LA0DG-GP
71.00773.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
SB
-1
-2
U16B
2 OF 2
KBC
PS/2
FIU
WPCE773LA0DG-GP
X3
X-32D768KHZ-34GPU
82.30001.661
82.30001.B21
SRN10KJ-6-GP
84.T3906.A11
2ND = 84.03906.F11
3RD = 84.03906.P11
CH731UPT-GP
83.R0304.A8H
2ND = 83.R2002.B8E
3RD = 83.R3004.A8E
GREEN ADAPTER CIRCUIT
Q4
NDS0610-NL-GP
84.00610.C31
TP0610K-T1-GP
83.2R004.081
SDM20E40C-7-F-GP
Q5
84.2N702.D31
2ND = 84.2N702.E31
2N7002E-1-GP
Q7
2N7002EDW-GP
84.27002.G3F
D16
RB751V-40-2-GP
83.R2004.B8F
83.R0304.A8F
D14
RB751V-40-2-GP
83.R2004.B8F
83.R0304.A8F
D21
MMPZ5232BPT-GP-U
MMBT3906-4-GP
G64
GAP-OPEN
PlanarID
-2: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC775
Size A2
Document Number JM41 Discrete
Rev -2
Date: Wednesday, May 06, 2009
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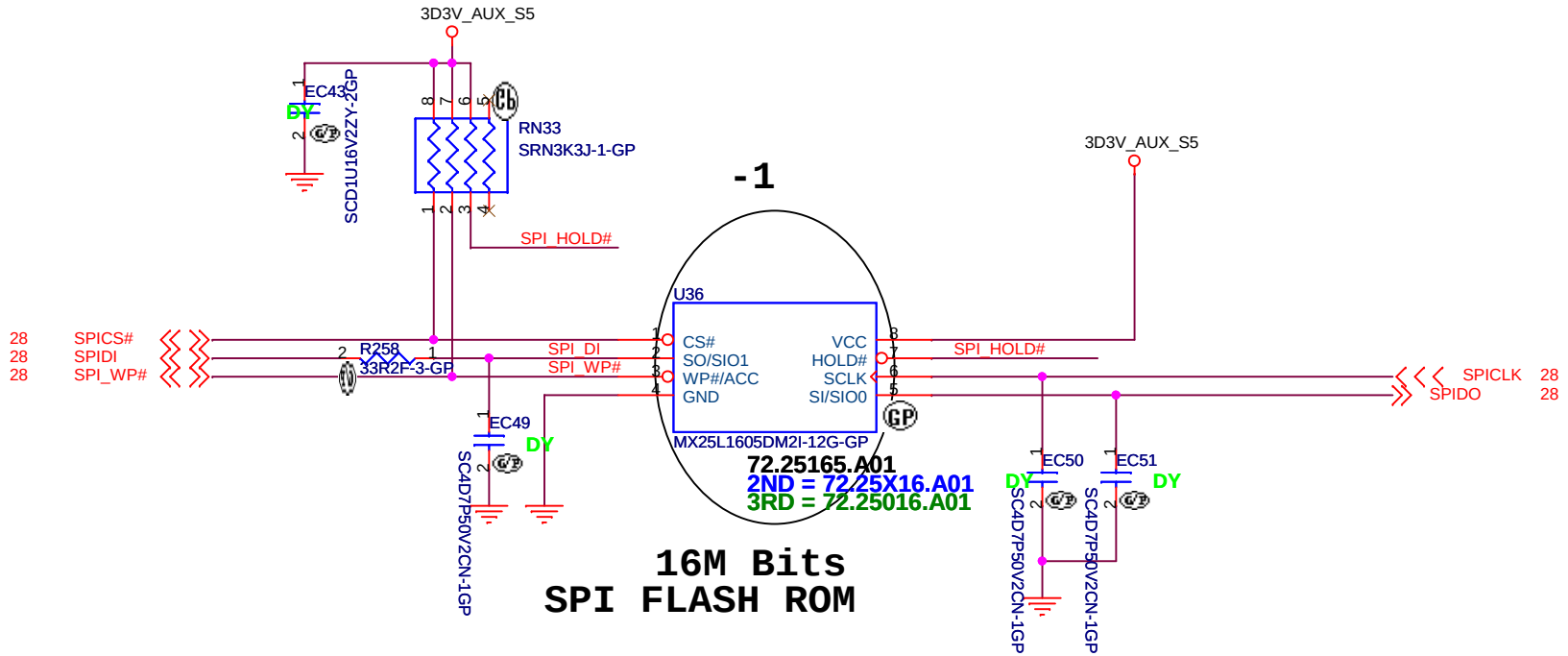
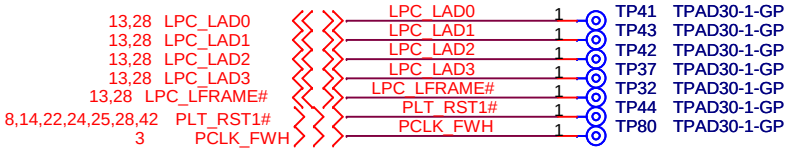
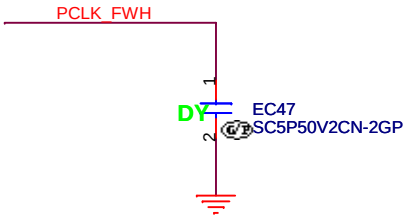


GOLDEN FINGER FOR DEBUG BOARD





DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
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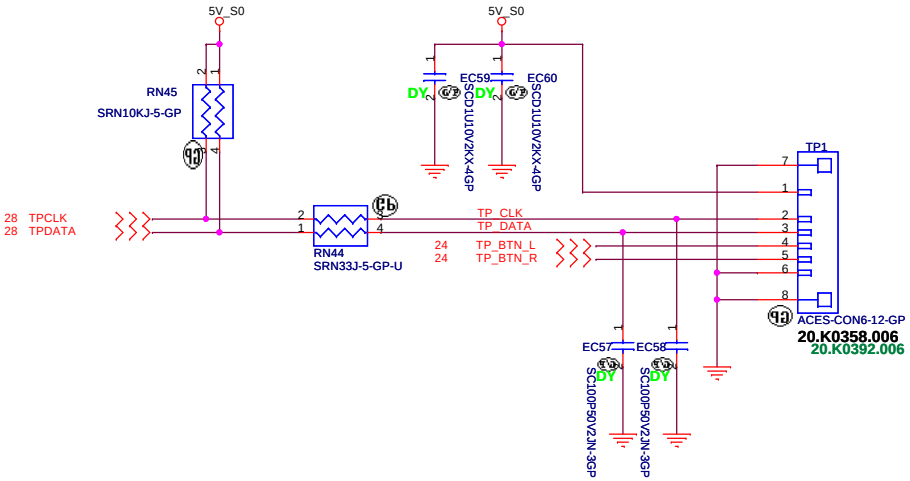
TOUCH PAD



DIS

緯創資通 **Wistron Corporation**
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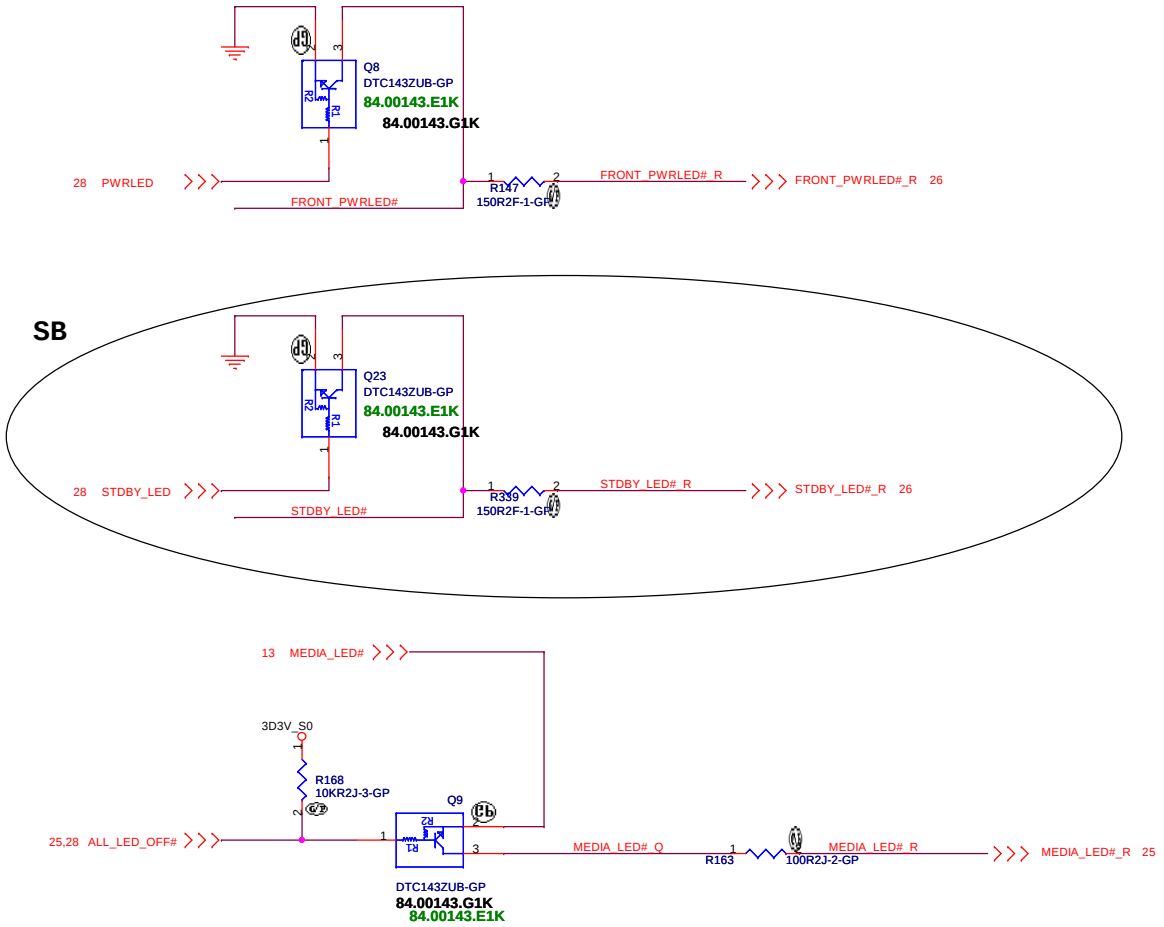
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Touch PAD*	
Size	Document Number: JM41_Discrete	Rev: -2
Date: Tuesday, April 28, 2009	Sheet 30 of 48	



DIS

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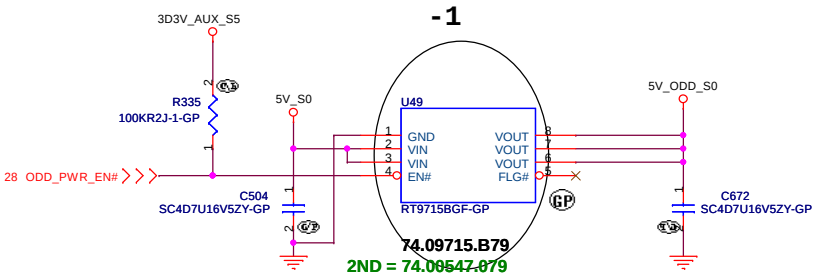
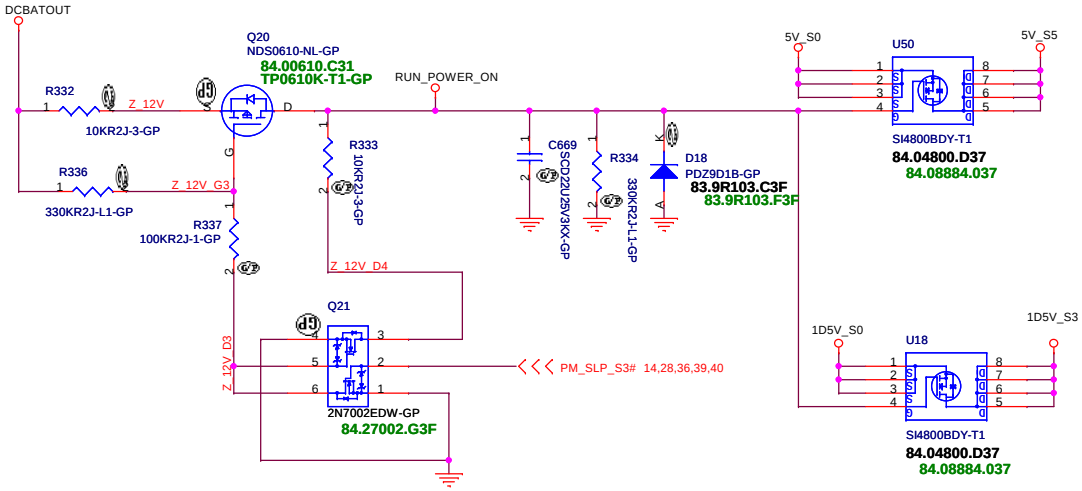
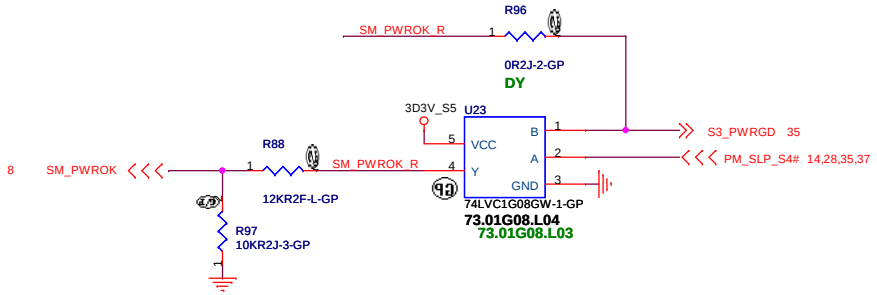
Title	**LED**	
Size	Document Number **JM41_Discrete**	Rev -2
Date: Tuesday, April 28, 2009	Sheet 31 of 48	

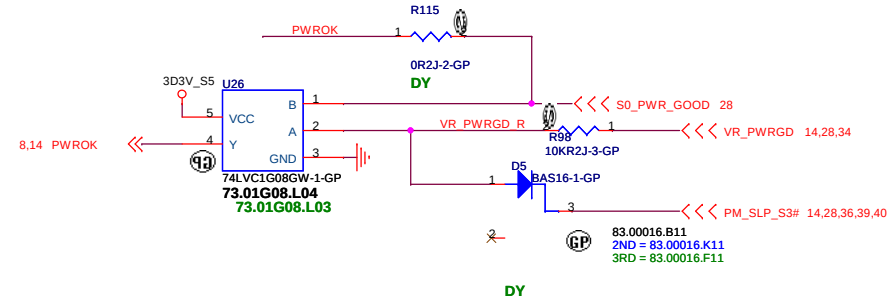
ODD Power

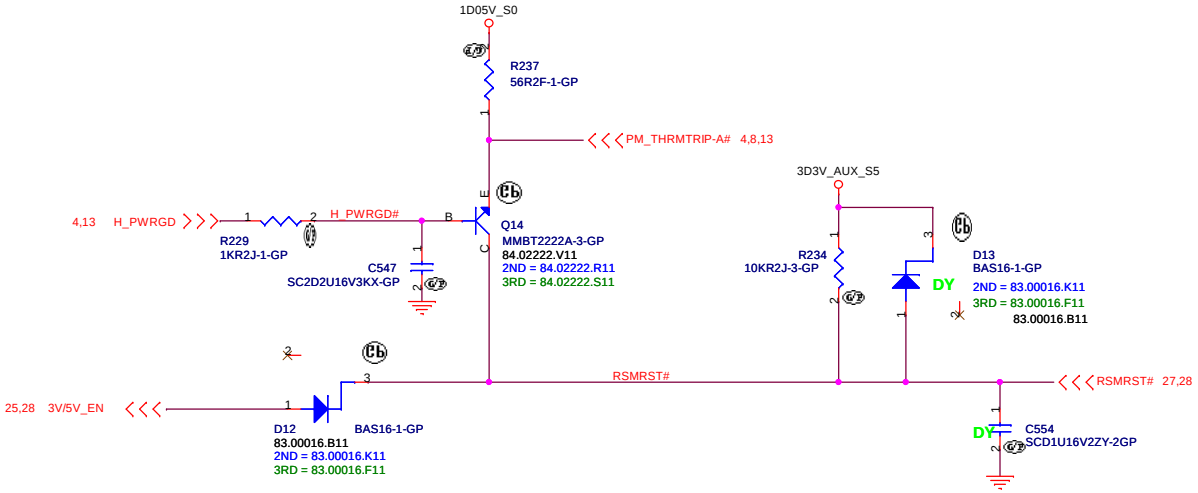


Run Power









DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN & ODD POWER	
Size	Document Number	Rev
	JM41_Discrete	-2
Date: Tuesday, April 28, 2009	Sheet 32 of 48	

CPU_CORE
ISL6261A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VR_PWROK

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=18A)

RT8202 1D05V_S0

DCBATOUT_8202_1D05V
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (10A)
CPUCORE_ON

RT8202 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (11A)
CPUCORE_ON

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_6263A

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

CPUCORE_ON

Output Power
VGFXCORE (O)

VCC_GFXCORE(7A)

RT9026 0D9V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

Charger MAX8731A

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA

BT+
DCBATOUT

TPS51125
5V/3D3V

DCBATOUT_51125

S5_ENABLE

ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

DIS

緯創資通 Wistron Corporation
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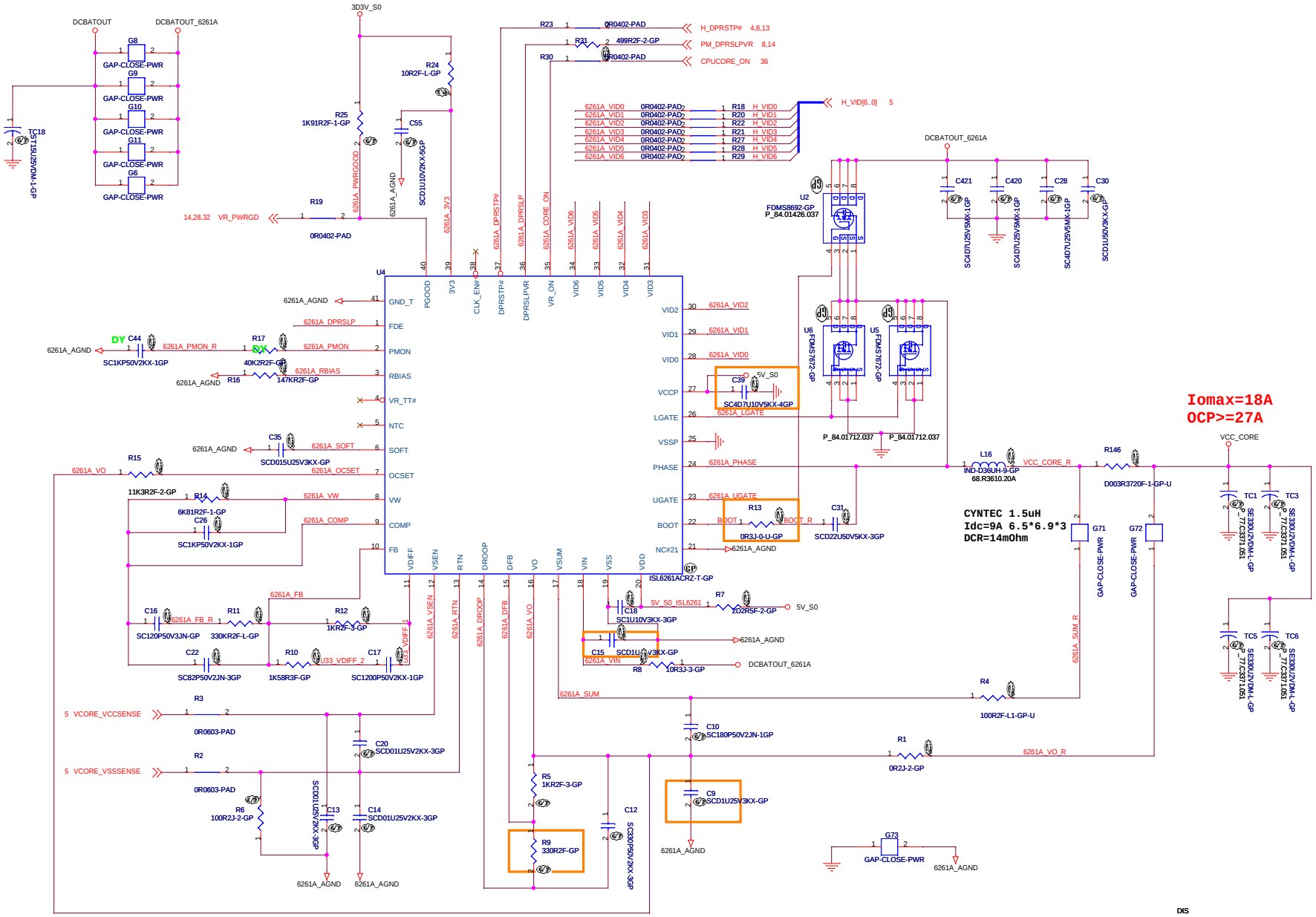
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size: B | Document Number: **JM41_Discrete** | Rev: -2

Date: Tuesday, April 28, 2009 | Sheet 33 of 48

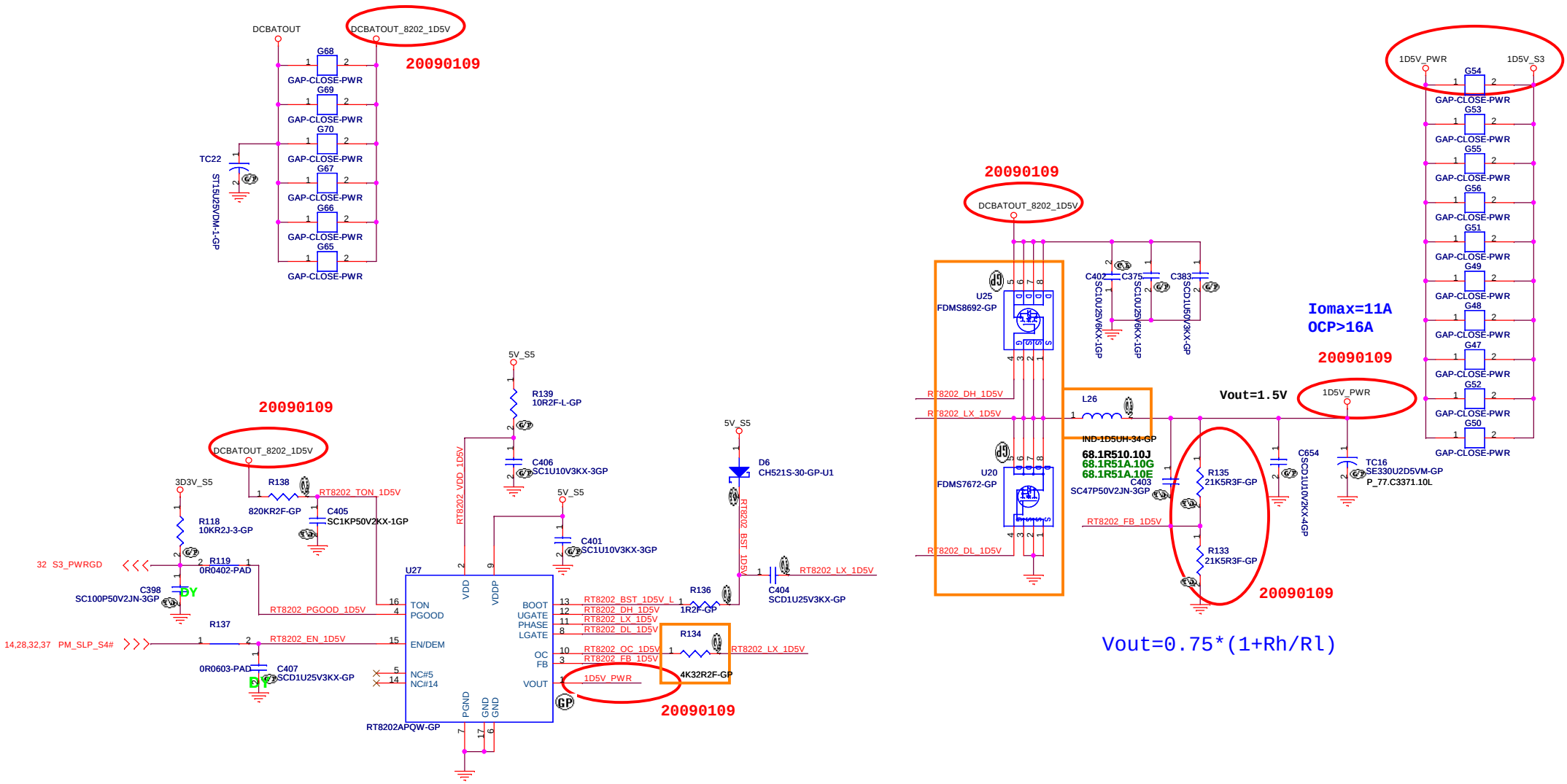


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6261A CPU CORE

Size	Document Number	Rev
Custom	JM41 Discrete	-2

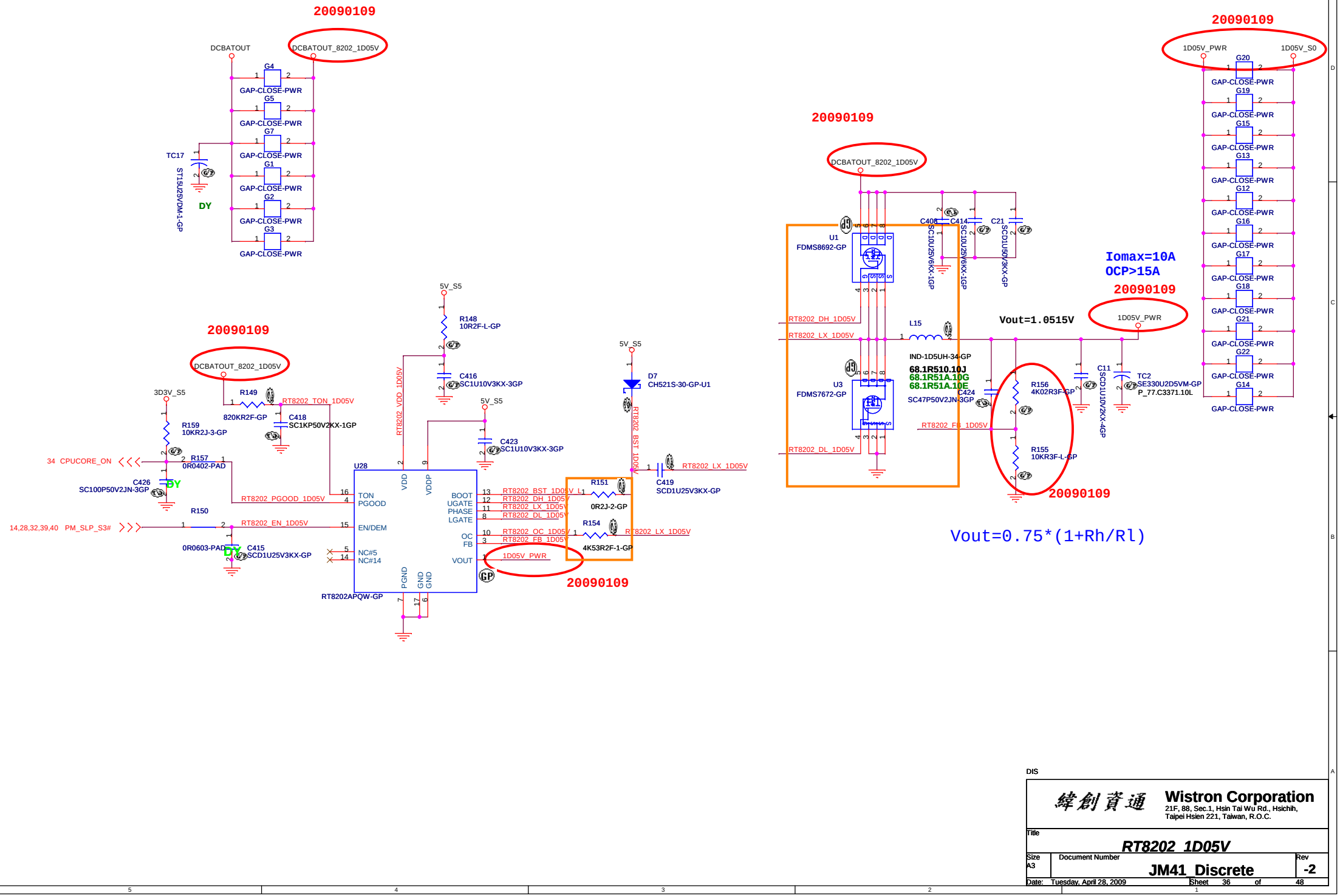
Date: Tuesday, April 28, 2009 Sheet 34 of 48



DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8202_1D5V***	
Size: A3	Document Number: **JM41_Discrete**	Rev: -2
Date: Tuesday, April 28, 2009	Sheet 35 of 48	

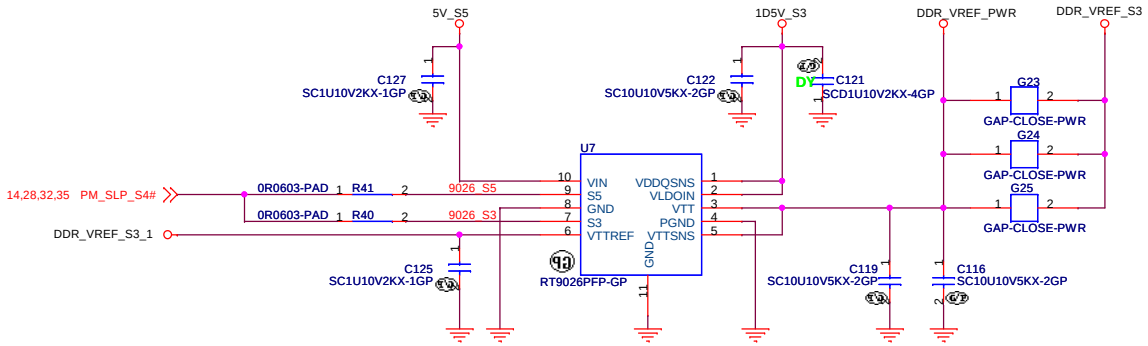


DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8202_1D05V***	
Size A3	Document Number **JM41_Discrete**	Rev -2
Date: Tuesday, April 28, 2009	Sheet 36 of 48	

Iomax=1.2A
OCP>2A



DIS

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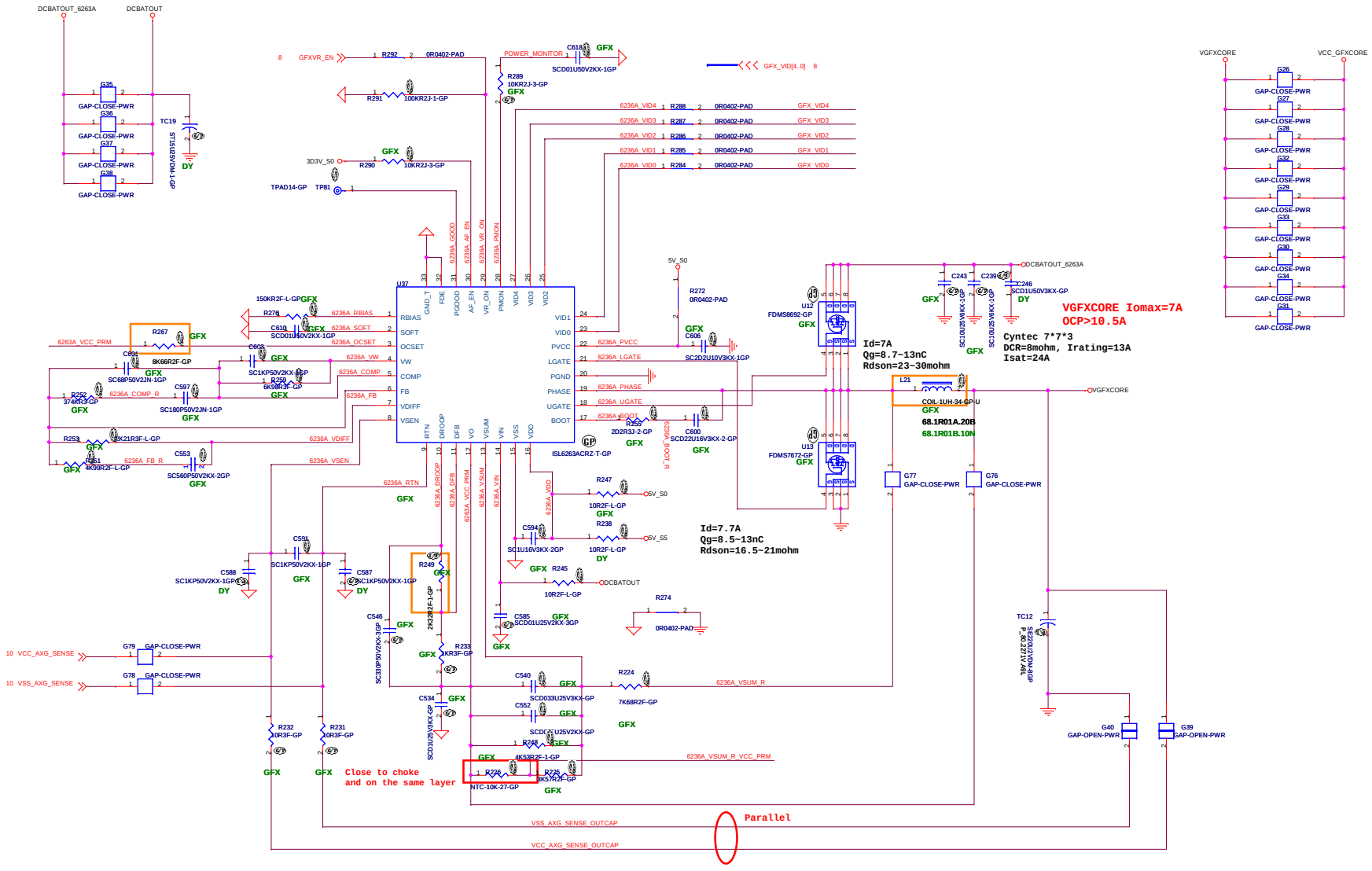
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT9026_0D75V***	
Size A3	Document Number **JM41_Discrete**	Rev **-2**
Date: Tuesday, April 28, 2009	Sheet 37 of 48	



DIS

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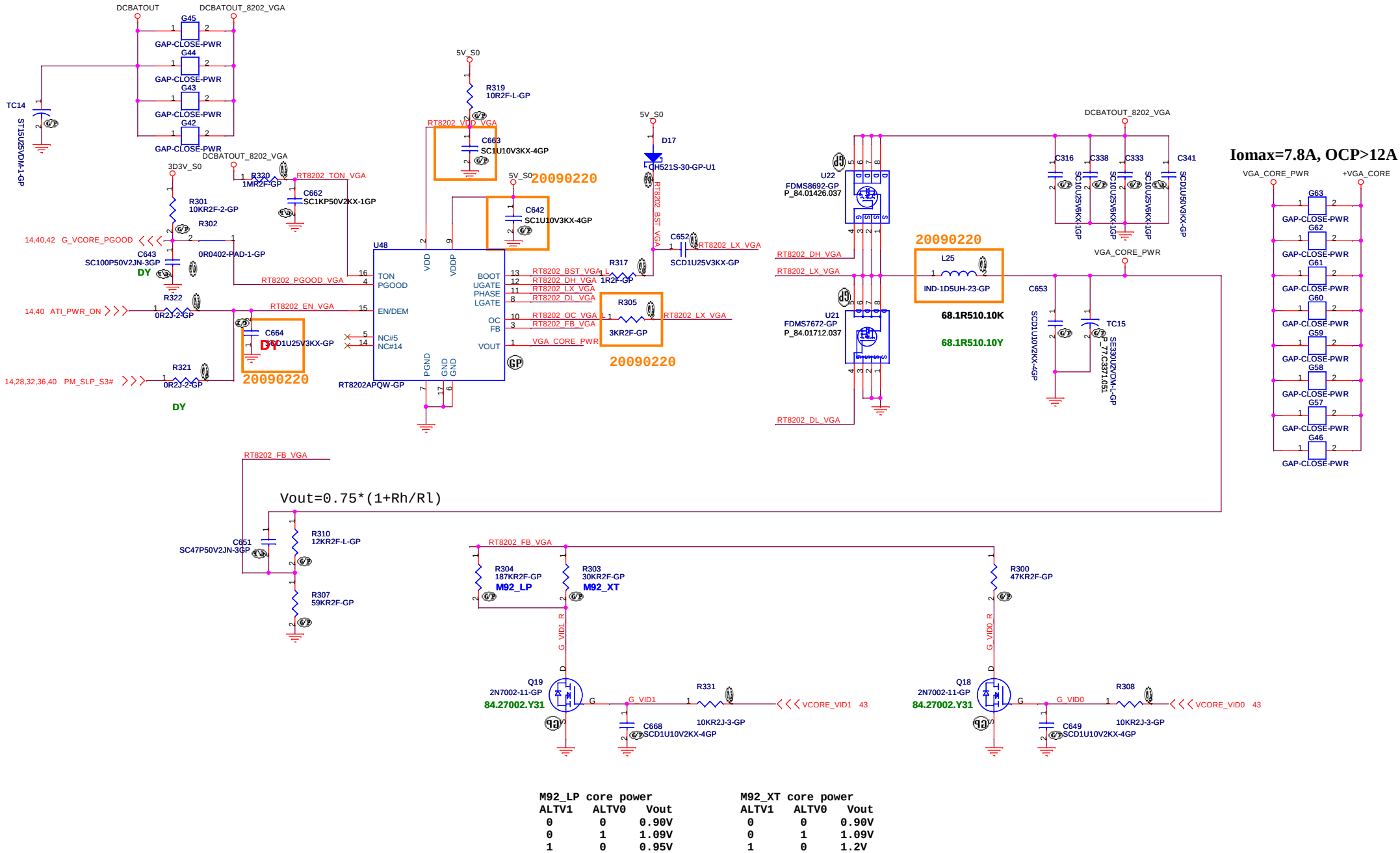
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ISL6263A_GFX CORE***

Size	Document Number	Rev
A2	JM41_Discrete	-2

Date: Tuesday, April 28, 2009 Sheet 38 of 48



M92_LP core power

ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	0.95V

M92_XT core power

ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

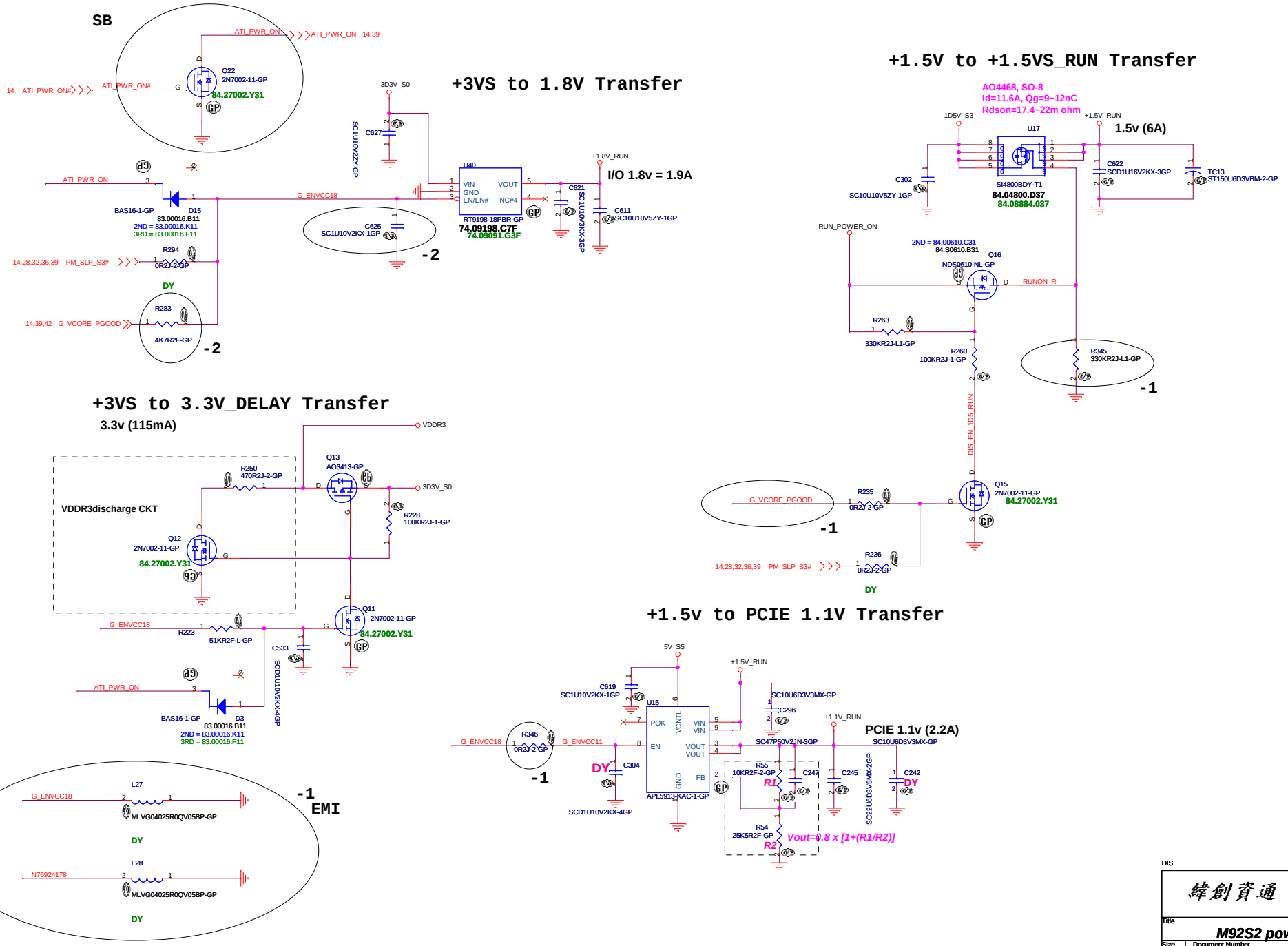
DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8202A VGA CORE**

Size: A3 | Document Number: **JM41 Discrete** | Rev: -2

Date: Thursday, April 30, 2009 | Sheet 39 of 48



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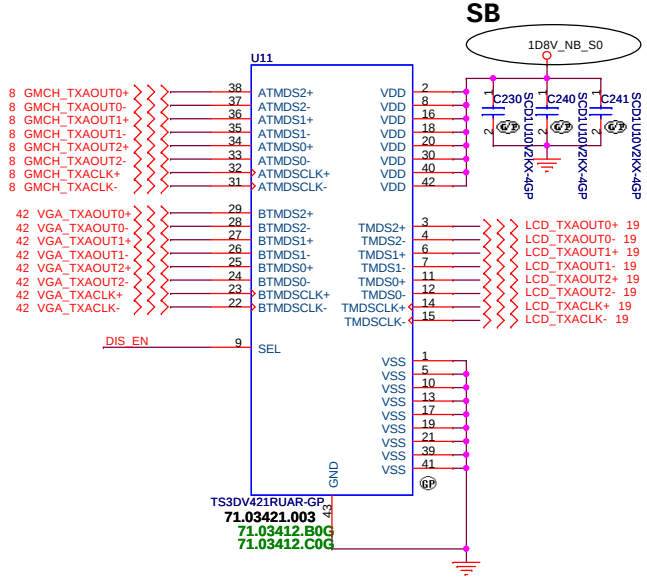
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M92S2 power***

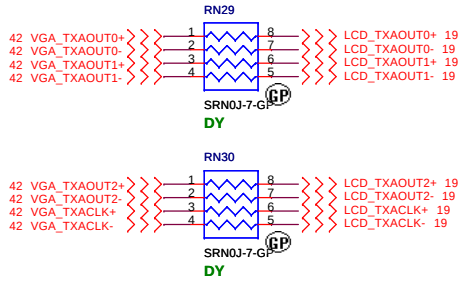
Size	Document Number	Rev
Custom	JM41_Discrete	-2
Date: Thursday, April 30, 2009	Sheet 40 of 48	

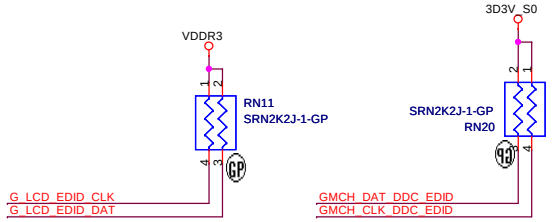
SB

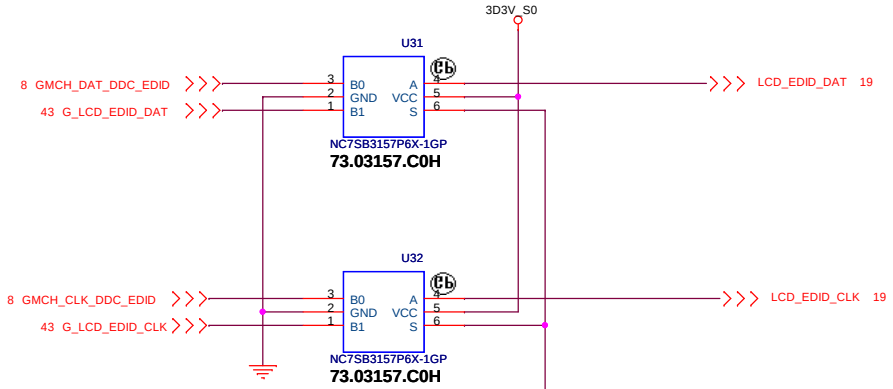


FUNCTION TABLE

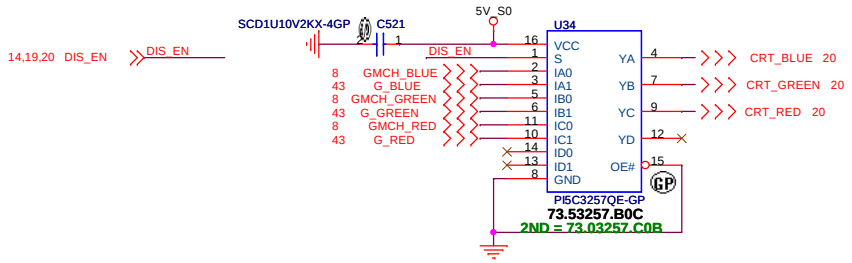
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

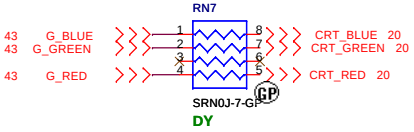






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

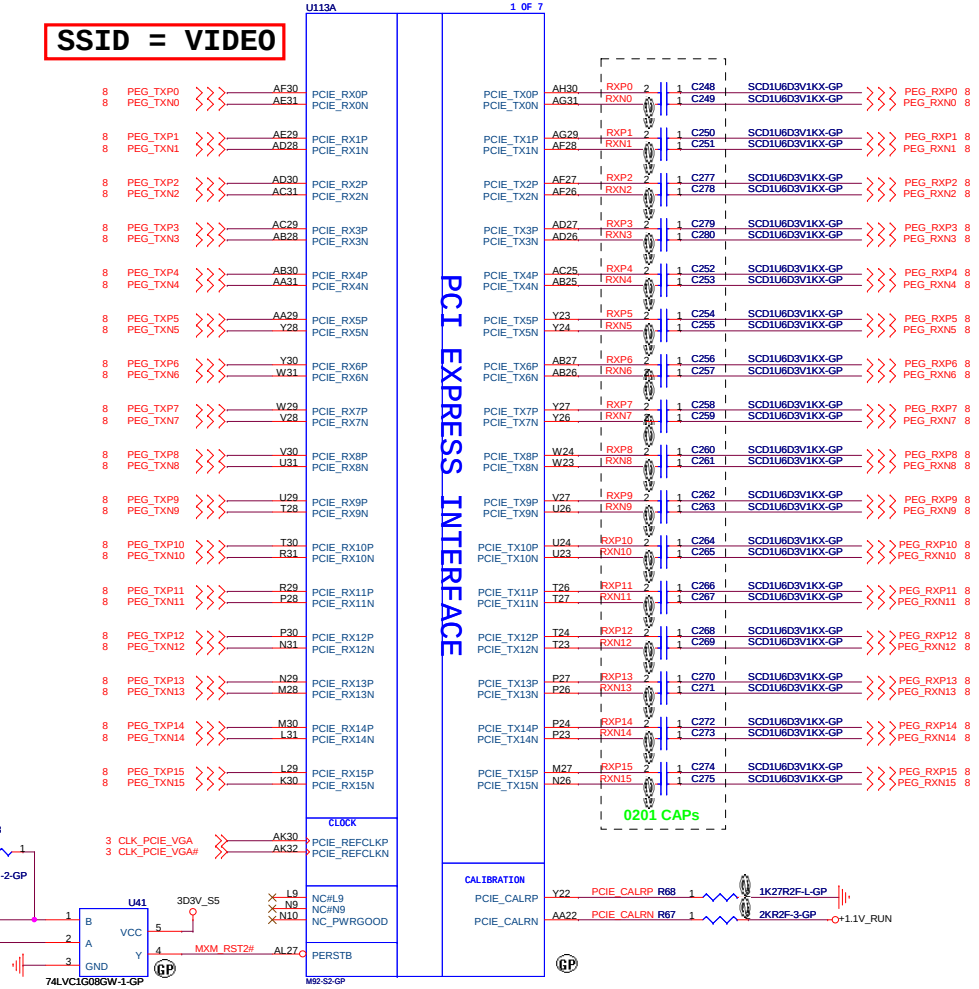


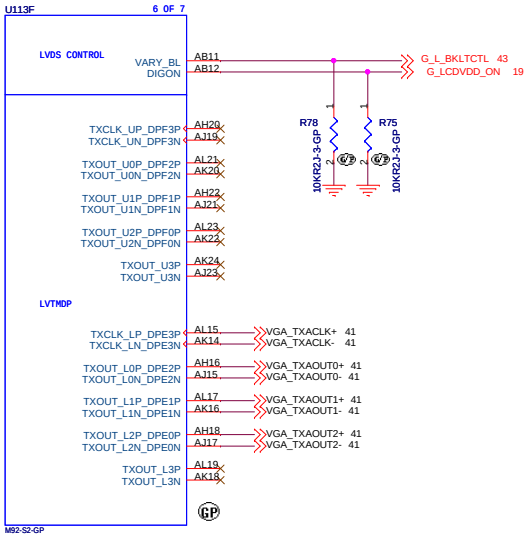


DIS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PX_SWITCH	
Size A3	Document Number	Rev -2
Date: Tuesday, April 28, 2009	Sheet 41 of 48	

SSID = VIDEO





DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VGA-PCIE/LVDS(1/4)***

Size	Document Number	Rev
Custom	JM41_Discrete	-2

Date: Tuesday, April 28, 2009 Sheet 42 of 48

SSID = VIDEO

DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung V

HDMI(DPA)

PLACE THESE CAPACITOR CLOSE TO CONNECTOR

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

CRT

(Placed between this pin and AVSSQ)

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG_IN

Wistron Corporation
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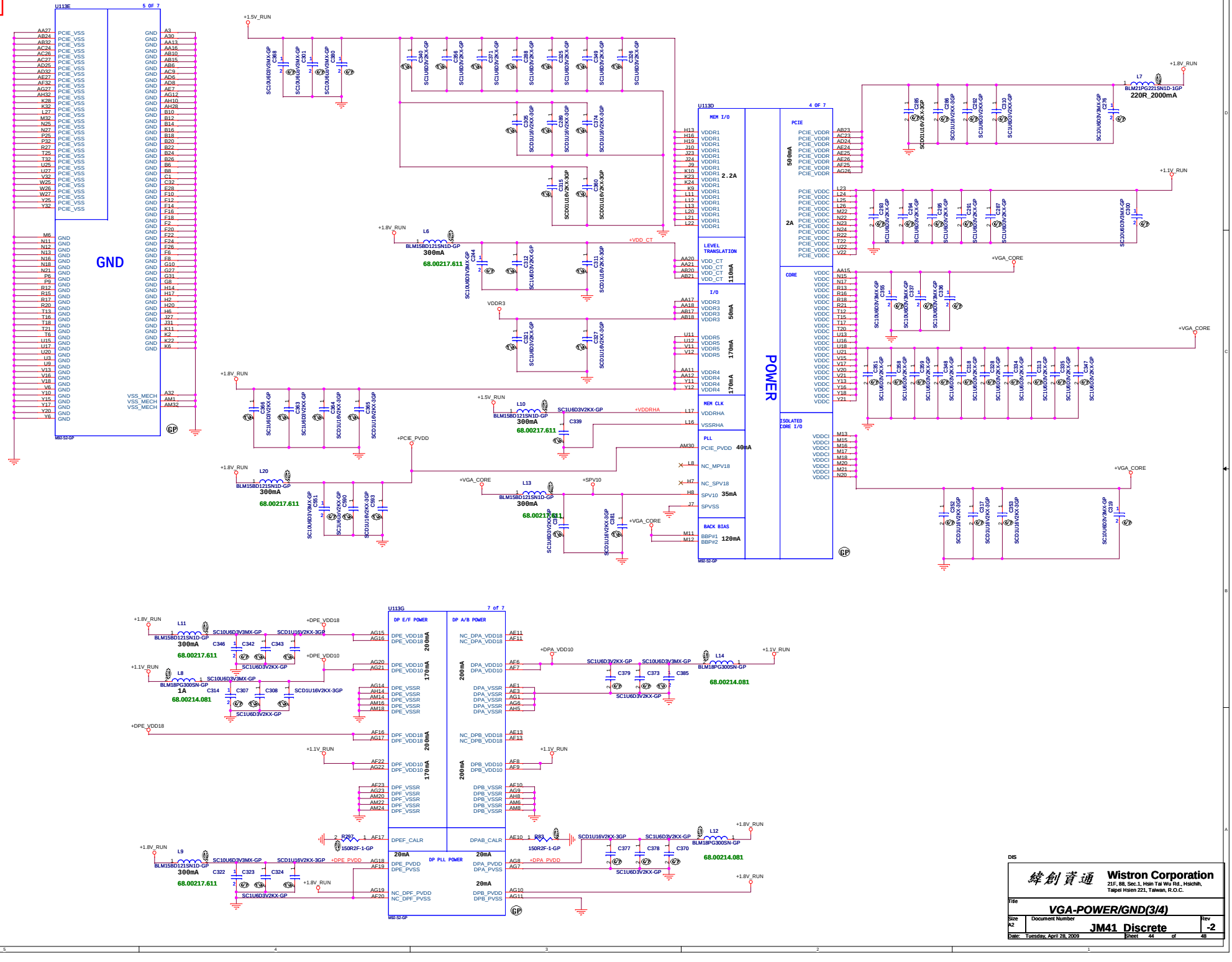
Title: VGA-TV/CRT/DP PORT(2/4)

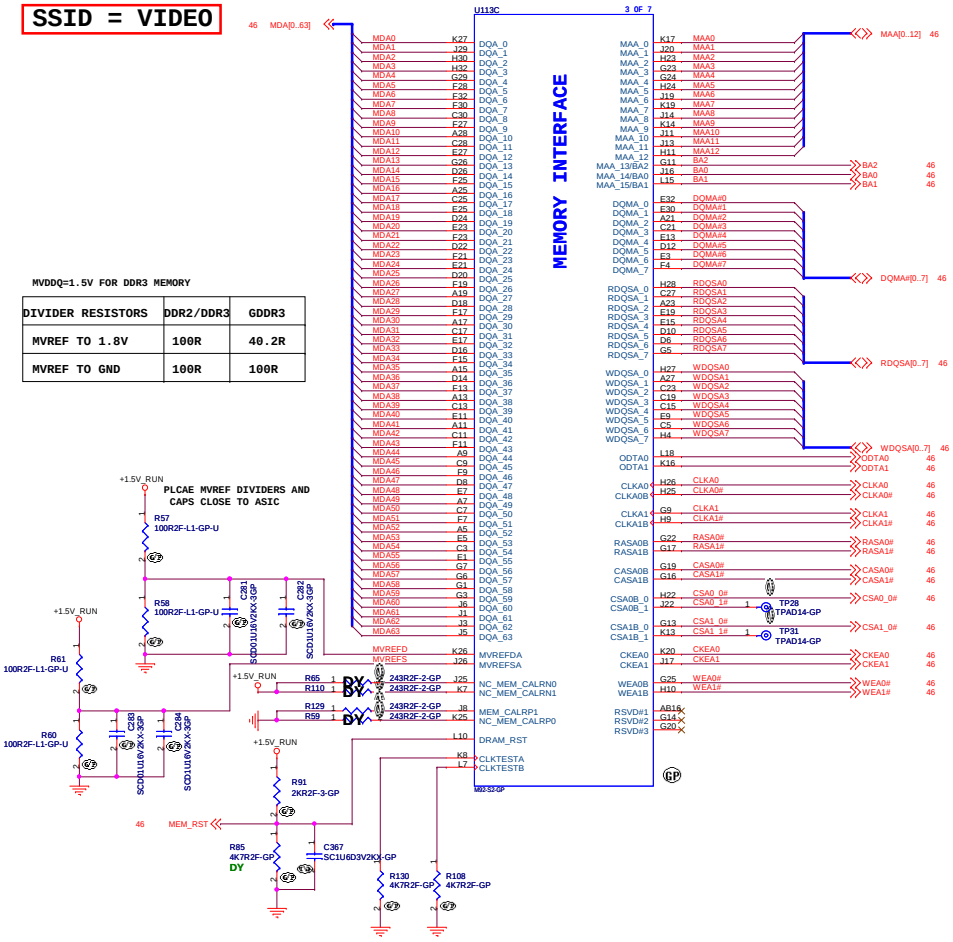
Size: C | Document Number: JM41_Discrete | Rev: -2

Date: Tuesday, April 28, 2009 | Sheet 43 of 48

SSID = VIDEO

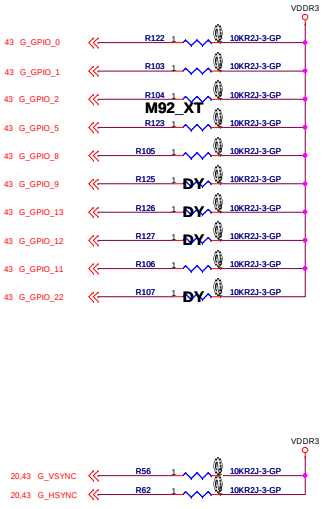

U113E
5 OF 7
GND
U113D
4 OF 7
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
CORE
ISOLATED CORE I/O
POWER
U113G
7 OF 7
DP E/F POWER
DP A/B POWER
DP PLL POWER
+1.5V_RUN
+1.8V_RUN
+1.1V_RUN
+VGA_CORE
+VDD_CT
+VDDRHA
+PCIE_PVDD
+SPV10
+DPA_VDD10
+DPE_VDD18
+DPE_VDD10
+DPE_PVDD
+DPA_PVDD
VDDR3
220R_2000mA
2.2A
500mA
2A
1.1A
300mA
170mA
200mA
50mA
40mA
35mA
120mA
68.00217.611
68.00214.081
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA-POWER/GND(3/4)
JM41_Discrete
-2
Tuesday, April 28, 2009
Sheet 44 of 48

SSID = VIDEO



MVDDQ=1.5V FOR DDR3 MEMORY

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

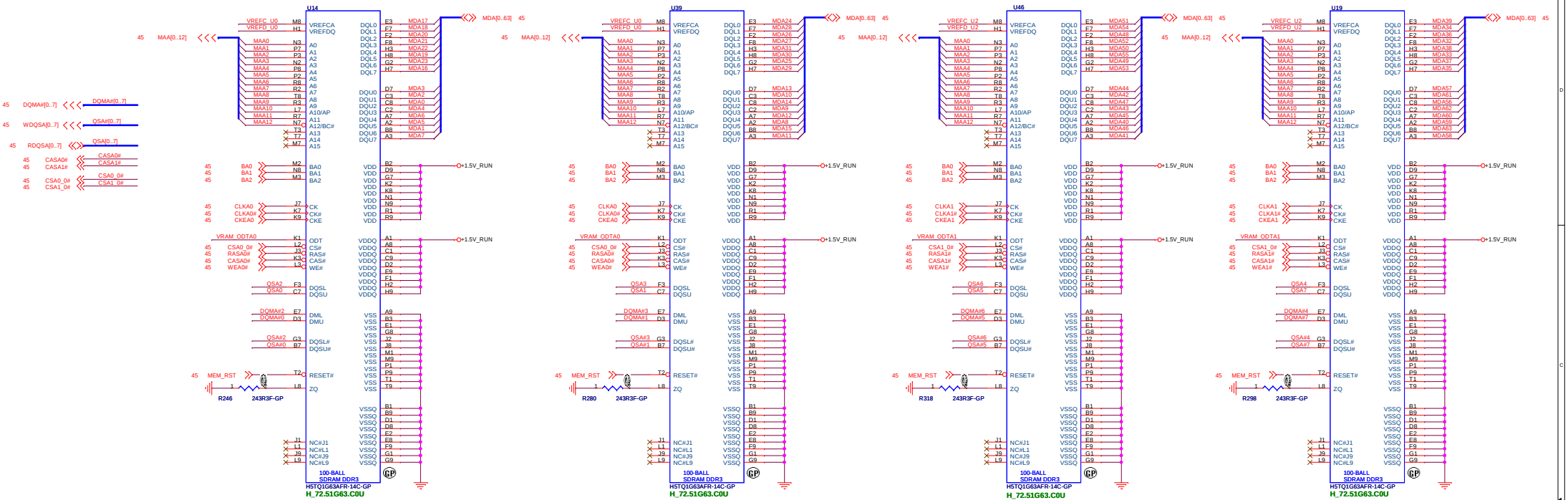
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
V 64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

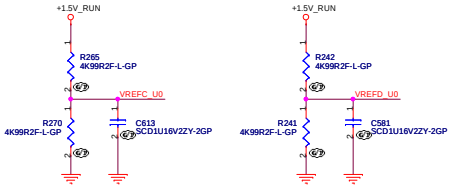
STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable 0= 50% Tx output swing V 1= Full Tx output swing
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled V 1= Tx de-emphasis enabled
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ#power management capability V 1= Enable CLKREQ# power management capability
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI V

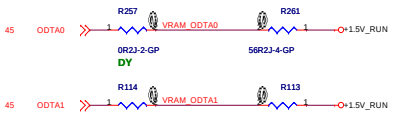
DIS

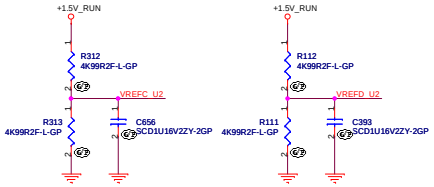
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VGA-MEMORY/STRAPS(4/4)		
Size: A2	Document Number: JM41 Discrete	Rev: -2
Date: Tuesday, April 28, 2009	Sheet 45 of 48	

512MB DDR3



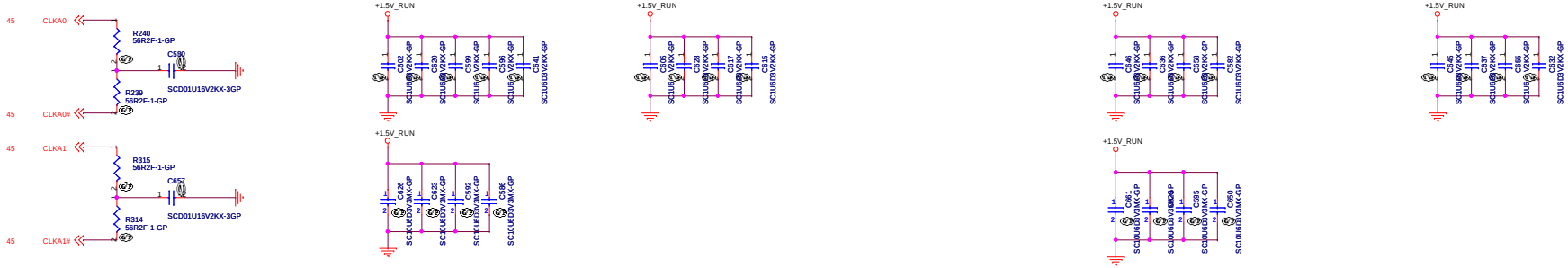






Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C



DIS

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Title	***VRAM***	
Size A2	Document Number **JM41 Discrete**	Rev -2
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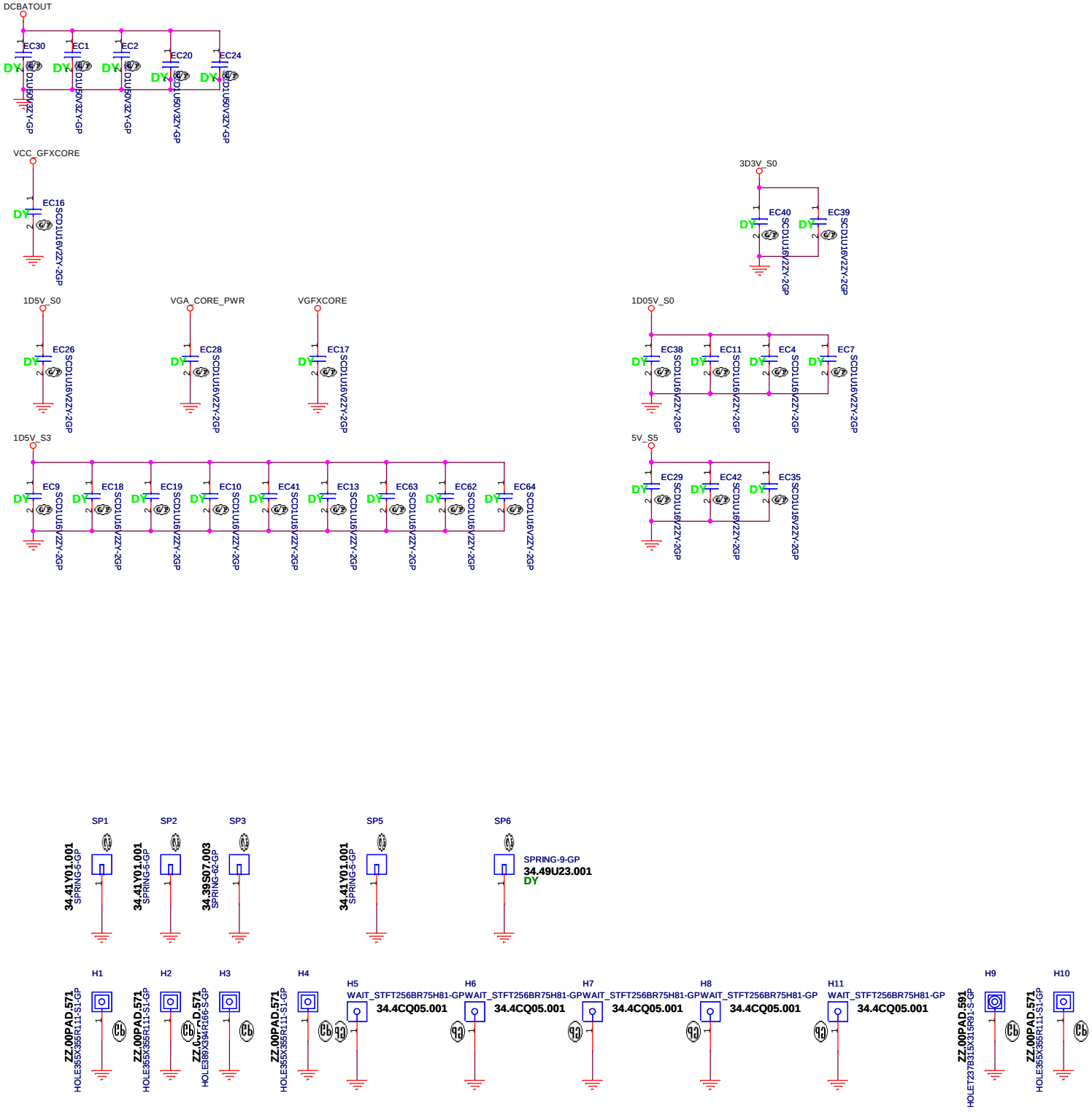

DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

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JM41/JM51 DIS Schematic EC Tracking Record
EC #/ Page / Description / Part Affected

EC SC01/11/connect NB1.A31 to GND(For power save)
EC SC02/14/net DIS_EN pull high 10K to 3D3V_S0
EC SC03/20/CN2.pin35 change to AGND
EC SC04/22/R311 change to 39.2K
EC SC05/22/U24.pin2 change to AGND
EC SC06/26/BTB2.pin9 add stand by led control signal
EC SC07/28/U16.pin66 add stand by led control signal
EC SC08/28/add circuit to support green adapter
EC SC09/28/net EJECT_BTN pull high 10K to 3D3V_S0
EC SC10/31/add circuit to stand by led control
EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
EC SC12/41/change U11 power plane to 1D8V_NB_S0

DIS

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Title: ***HISTORY***

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